

CONTENT

ADSP MEMORY MAP

ADSP MEMORY MAP - SHORT FORM

TIMING ADSP 2100 - SYSTEM 4 BOARD

PARTS LIST SPECIFICATION:

ASSY, SUB, DRIVER ADSP - D.SIMU. - REV/B

SCHEMATIC DRIVER ADSP - REV/B

PARTS LIST SPECIFICATION:

ASSY, SUB, ADSP II PCB - H.D. - REV/C

ASSY, ADSP II PCB - H.D. COMP. - REV/B

ASSY, ADSP II PCB - H.D. RACE - REV/C

ASSY, ADSP II PCB - R. D. PANO. - REV/A

FABRICATION ADSP II - REV/A

ASSEMBLY ADSP II - REV/C

SCHEMATIC ADSP II PCB - REV/C

Driver ADSP Board, Rev 1
Uses ADSP-2100 Rev 3
68010 Stuff:

5/13/87

Program Memory:

To Access Program Memory Set Flag ADSPBR Low.
Program Memory is accessed as 8K Longwords with the low 24 bits used.
Set Flag ADSPBR High.

The ADSP Program Memory is accessible immediately after setting
ADSPBR Low.

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Data Memory:

To Access Data Memory Set Flag ADSPBR Low.
Data Memory is accessed as 8K Words.
Set Flag ADSPBR High.

The ADSP Data Memory is accessible immediately after setting
ADSPBR Low.

===

Sequential Output Memory:

Set /BCON Low - The 68010 sees Sequential Output Memory #1.
The ADSP-2100 sees Sequential Output Memory #2.

Set /BCON high - The 68010 sees Sequential Output Memory #2.
The ADSP-2100 sees Sequential Output Memory #1.

=====

ADSP Memory Map

Program Memory 0000 - 1FFF (8K x 24)

a Memory 0000 - 1FFF (8K x 16)

2000 SIMBUF Read the Sequential Input Memory; Increment the Address.

It is necessary to follow a SIMBUF read with two NOPs (or other instructions) before doing another SIMBUF read.

2001 SIMLD Write Data to Sequential Input Memory Address Counter

It is necessary to follow a SIMLD write with two NOPs (or other instructions) before doing a SIMBUF read.

2002 SOMD Write Data to Sequential Output Memory; Increment Address

It is necessary to follow a SOMD write with one NOP (or other instruction) before doing another SOMD write.

2003 SOMLD Write Data to Sequential Output Memory Address Counter

2005 XOUT Write D0 to Latch which can be read by 68010

2006 GINT Generate 68010 Interrupt 2

2007 MPAGE Write DMD0 to Memory Page Select (For Sequential Input Memory)

- Notes:
1. 2000 and 2004 must be READ only.
 2. 2001, 2002, 2003, 2005, 2006, and 2007 should be WRITTEN to only.
 3. The Sequential Input Memory consists of two 64K Word Pages, Selected by MPAGE. Sequential access will not cross the page.
 4. The Sequential Output Memory is actually two independent memories. The 68010 selects which one is used by whom.

ADSP Memory Map - Short Form

Program Memory 0000 - 1FFF (8K x 24)

Data Memory 0000 - 1FFF (8K x 16)

2000 SIMBUF Read the Sequential Input Memory; Increment the Address.

It is necessary to follow a SIMBUF read with two NOPs (or other instructions) before doing another SIMBUF read.

2001 SIMLD Write Data to Sequential Input Memory Address Counter

It is necessary to follow a SIMLD write with two NOPs (or other instructions) before doing a SIMBUF read.

2002 SOMD Write Data to Sequential Output Memory; Increment Address

It is necessary to follow a SOMD write with one NOP (or other instruction) before doing another SOMD write.

2003 SOMLD Write Data to Sequential Output Memory Address Counter

2005 XOUT Write D0 to Latch which can be read by 68010

2006 GINT Generate 68010 Interrupt 2

2007 MPAGE Write DMD0 to Memory Page Select (For Sequential Input Memory)

- Notes:
1. 2000 and 2004 must be READ only.
 2. 2001, 2002, 2003, 2005, 2006, and 2007 should be WRITTEN to only.
 3. The Sequential Input Memory consists of two 64K Word Pages, Selected by MPAGE. Sequential access will not cross the page.
 4. The Sequential Output Memory is actually two independent memories. The 68010 selects which one is used by whom.

Timing For ADSP-2100 System 4 Board

1 of 4

Using Data Sheet for Revised ADSP-2100, August 22, 1986
d Margolin 7/7/86, 7/17/86, 7/29/86, 8/25/86

Old Memory Reads:

Program Memory Address (PMA) Valid to Program Memory Data (PMD) required = 50 ns

Therefore, Program Memory Access Time: 50 ns

Data Memory Address (DMA) Valid to Data Memory Data (DMD) required = 57 ns
Therefore, Data Memory Access Time: 57 ns

New Memory Reads:

Program Memory Address (PMA) Valid to Program Memory Data (PMD) required = 50 ns
Therefore, Program Memory Access Time: 50 ns

RAM access = 50 ns - 5 ns (Address Decoding) = 45 ns max

Data Memory Address (DMA) Valid to Data Memory Data (DMD) required = 57 ns
Therefore, Data Memory Access Time: 57 ns

RAM access = 57 ns - 10 ns (Address Decoding) = 47 ns max

New Signals:

Data Memory Select (/DMS), same timing as DMA, usable as chip select.

Program Memory Select (/PMS), same timing as PMA, usable as chip select.

Program Memory Read (/PMRD), Read Strobe, usable as output enable.
(Note: Fast RAMs do not have a separate output enable.)

PMA Valid to /PMRD Low = 10 ns min
/PMRD Low to PMD Required = 37 ns max
/PMRD High to PMA Invalid = 16 ns

/PMRD Width = 49 ns min

Data Memory Read (/DMRD), Read Strobe, usable as output enable
(Note: Fast RAMs do not have a separate output enable.)

DMA Valid to /DMRD Low = 16 ns
/DMRD Low to DMD Required = 40 ns max
/DMRD High to DMA Invalid = 16 ns

/DMRD Width = 49 ns min

Old Memory Writes:

DMD Out Valid to /DMWR High = 28 ns min
PMD Out Valid to /PMWR High = 20 ns min

New Memory Writes:

ID Out Valid to /DMWR High = 28 ns min
 ID Out Valid to /PMWR High = 20 ns min

=====
Memory Requirements:

Tacc = 45 ns min
 Address Setup to Write Start = 0 ns
 Write Pulse Width = 49 ns
 Data Set up to end of Write = 20 ns max

=====
Cypress 45 ns RAM (CY7C168):

Program Memory Access Time: 50 ns
 5 ns memory select + 45 ns RAM access = 50 ns (ok)

Data Memory Access Time: 57 ns
 9 ns memory select + 45 ns RAM access = 54 ns (ok)

Program Memory Write pulse: 49 ns
 RAM Write pulse = 35 ns (ok)

Data Memory Write pulse = 49 ns
 RAM Write pulse = 35 ns (ok)

Data Valid to End of Write = 28 ns DM
 Data Valid to End of Write = 20 ns PM

RAM Data Setup to End of Write = 15 ns min (ok)

Data Hold = 22 ns
 RAM requirement = 3 ns (ok)

Program Memory Address Setup to Start of Write = 4 ns min
 Data Memory Address Setup to Start of Write = 6 ns min
 RAM requirement = 0 ns (ok)

Program Memory Address Setup to End of Write = 59 ns min
 Data Memory Address Setup to End of Write = 64 ns min
 RAM requirement = 35 ns

=====
 After the ADSP reads the Sequential Input Memory (SIMBUF) and increments the EPROM address, the next memory access has to wait at least 216 ns before it can be read again. [ALS169 = 16ns + 27256 200ns].

For a SIMBUF read followed by a NOP followed by another SIMBUF read:
 Start at end of SIMBUF: ALS169 = 16ns, 27256 = 200ns, LS244 = 18 ns.
 Total is 234 ns. The data is therefore available 16 ns before the end of the second SIMBUF read. The data must be stable 3 ns before Clk 7/8. The signal that increments the ALS169s is 1 half-clock plus gate delays after Clk 7/8 for total of ~26 ns. The Data must be available 29ns less than 2 major cycles or 221ns. This would require EPROM with 221-16-18 = 187ns.

It is therefore necessary to follow a SIMBUF read with two NOPs (or other instructions) before doing another SIMBUF read.

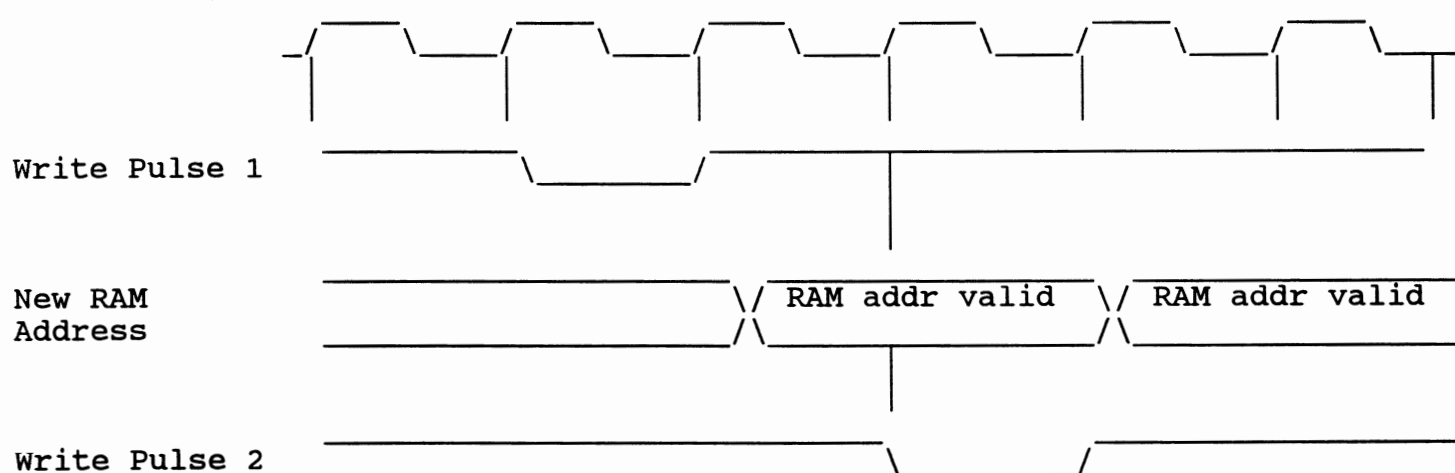
e alternative is to use 170ns EPROM.

==

After the ADSP writes to the Sequential Output Memory (SOMD) it must wait at least 1 Instruction cycle before writing to it again.

When it writes to it the Data is captured in a latch which extends the memory write until the end of the next instruction. (The ADSP can be doing another instruction). The Sequential Output Memory is then incremented. (The ALS569 takes 16 ns.)

Major Cycles: Write 1 NOP Write 2



=====

Bus Request (For Both Program and Data Memories):

BR is recognized during clock cycles 3/4 and tri-states the bus about 2 half-cycles after the next clock cycle 3/4. (about 150 ns total). If BR is asserted during clock cycles 4/5, this will add about 125 ns to the access time for a total of 275 ns worst case.

The 68010 should be able to Set ADSPBR Low and begin accessing memory with its next instruction.

=====

Nitty Gritty

/SIMBUF = Read the Sequential Input Memory and increment the Address Counter.

There is a worst case delay of 9.0 ns from Data Memory Address Valid to /SIMBUF. /DMS low to /DMRD low is 16 ns min, so there will not be any glitches on the clock low. The total delay from /DMRD low to the Counter Clock Input low is 'AS08 + 'AS32 = 9 ns.

/DMRD low to Data Memory Data In Required = 40 ns max
(LS244 prop delay is 18 ns max)

/DMRD high to Data Memory Address Invalid is 16 ns min. The Counter Clock Input will go high 9 ns after /DMRD high with no glitches.

=====

All of the decoded writes are strobed by /DMWR and are therefore delayed 8 ns coming and going.

/DMWR high to Address Invalid = 16 ns min
 /DMWR high to Data Out Invalid = 22 ns min

Therefore the Decoded Writes will go high with both address and data valid.

=====

/SIMLD = Write to the Sequential Input Memory Address Counter

/SIMCLK to load the counters will be delayed an additional 4 ns with no problem.

/SIMLD low will be valid 20 ns before /SIMLD. It will be at least 49 ns before /SIMCLK goes high. The ALS169 has a Load setup time of 15 ns.

=====

SOMLATCH = Write to the Sequential Output Memory Data Latch.

SOMLATCH is delayed 4 ns from the decoded write strobe with no problem.
 (The LS373 has 0 setup time and 10 ns hold time.)

/SOMD = SOMLATCH decoded address, is guaranteed to be valid when CLKOUT goes high. Generates an extended Memory Write for the 6264s.
 CLKIN low (7-8) to CLKOUT high is 8 - 19 ns.
 CLKIN high (8-1) to /DMS invalid is 14 ns min.
 CLKIN Low (7-8) to CLKIN high (8-1) is 15 ns so that CLKOUT high must occur (at the very latest) 3 ns after CLKIN high (8-1) which is 16 ns before /DMS invalid.

=====

/XIN = Read the Auxiliary Input Buffer (A decoded Read)

/XOUT = Write to the Auxiliary Output Latch (A Write Pulse)

/GINT = Generate a 68010 Interrupt (A Write Pulse)

/MP = Select the Memory Page (A Write Pulse)

=====

Title / ASSY, SUB, DRIVER ADSP		P/L A044421-01	Rev / B
GAMES ENGINEERING PARTS LIST SPECIFICATION	PROJECT: DRIVING SIMULATOR		Page 1 of 2



Drawn by: G. POPKIN	Next Assy:
Checked by: A. JACKSON	
Design Eng: JED MARGOLIN	Comp. Eng:
Proj. Eng: R. MONCRIEF	Mfg. Eng: WRIGHTINOUR
Ind. Design:	Qual. Eng:

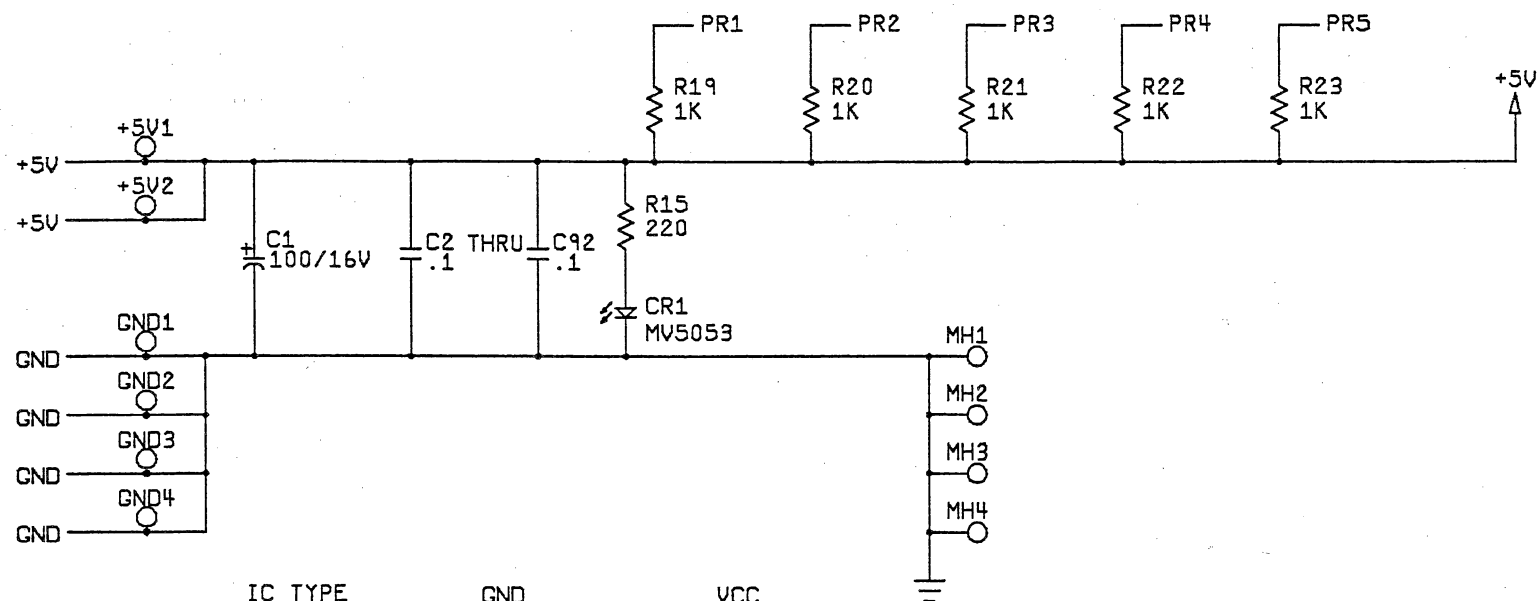
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A	PRODUCTION RELEASE	8/88					
B	ECN 13214 <i>6-0-1</i>	<i>12-2-88</i>	<i>9m RLM</i>				

ITEM	PART NO	QTY	Description	Ref. Designators
1	044422-01	1	P.C. Board	
2				
3				
4				
5	122002-104	91	CAP, .1μF, 50V, CER	C2-92
6	124008-107	1	CAP, 100μF, 16V, ELEC	C1
7				
8	179021-060	1	CONN, HDR, 60 CKT, 4 WALL, .1 X .1C	J1
9				
10	131027-002	3	DIODE, MV5053, LIGHT EMIT	CR1-3
11				
12				
13				
14	144008-002	1	IC, 32MHZ CLOCK MODULE	X1
15				
16				
17				
18				
19	110000-103	15	RES, 10K, 5%, 1/4W	R1-12, R16-18
20	110000-151	2	RES, 150, 5%, 1/4W	R13, R14
21	110000-102	5	RES, 1K, 5%, 1/4W	R19-23
22	110000-221	1	RES, 220, 5%, 1/4W	R15
23				
24				
25				
26	79-42C28	4	SOCKET, 28 PIN	10H, 10J, 10K, 10L
27	179236-001	1	SOCKET, IC, PGA, 101 CKT, LIF	ADSP2100
28				
29				
30	179051-001	6	TEST POINT	+5V1, +5V2, GND1-4
31				
32	137517-001	2	IC, 74ALS138	7B, 7C
33	137471-001	4	IC, 74ALS169	9L, 9K, 9J, 9H
34	137464-001	1	IC, 74ALS32	7A
35	137476-001	8	IC, 74ALS569	4A, 4B, 4C, 4D, 4E, 4F, 4H, 4J

Title / ASSY,SUB,DRIVER ADSP		P/L A044421-01	REV / B
GAMES ENGINEERING PARTS LIST SPECIFICATION		PROJECT: DRIVING SIMULATOR	Page 2 of 2

ITEM	PART NO	QTY	Description	Ref. Designators
36	137156-001	2	IC, 74ALS74	7L, 6K
37	137480-001	1	IC, 74AS00	8K
38	137433-001	1	IC, 74AS04	6L
39	137484-001	1	IC, 74AS08	5L
40	137522-001	2	IC, 74AS138	5K, 7J
41	137487-001	2	IC, 74AS32	6J, 8H
42	137038-001	13	IC, 74LS244	3C, 3D, 3E, 3F, 3K, 6C, 6D, 7D, 8C, 8D, 8F, 8J, 8L 1D, 1E, 2D, 2E, 6A, 6B, 8A, 8B, 8E
43	137134-001	9	IC, 74LS245	7K
44	37-74LS259	1	IC, 74LS259	1C, 1F, 2C, 2F
45	137143-001	4	IC, 74LS373	
46				
47				
48				
49	137537-003	20	IC, SRAM, 4KX4, (8168D45)	5A, 5B, 5C, 5D, 5E, 5F, 5H, 5J, 9A, 9B, 9C, 9D, 9E, 9F, 10A, 10B, 10C, 10D, 10E, 10F
50	137535-006	4	IC, SRAM, 8KX8, (6264D15)	1H, 3H, 1A/B, 3A/B

REVISIONS				
SYM	DESCRIPTION	DATE	INCORP	CHECK APPROVED
A	PRODUCTION RELEASE	7-18 1988	GRP	R.D. pm R.D.
B	ECN-13214	11-21 1988	LB F	G.P. sm



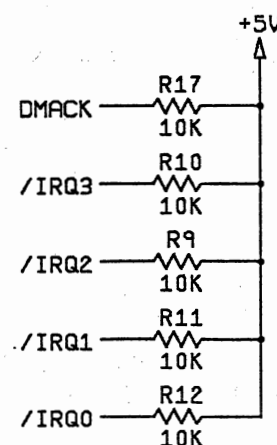
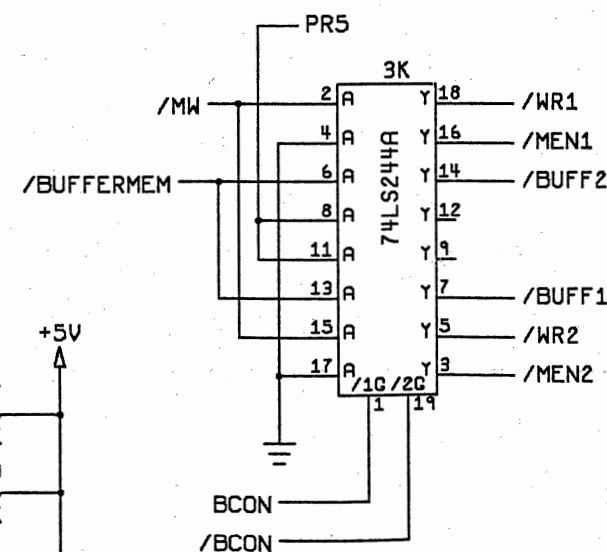
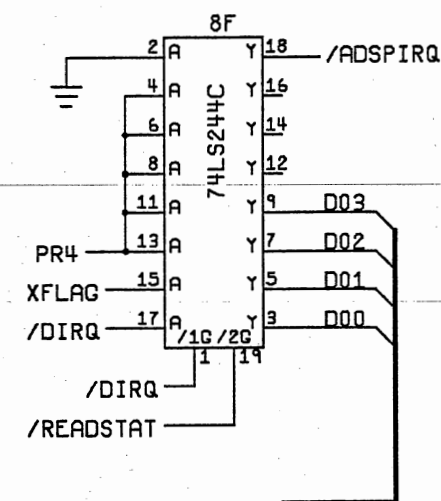
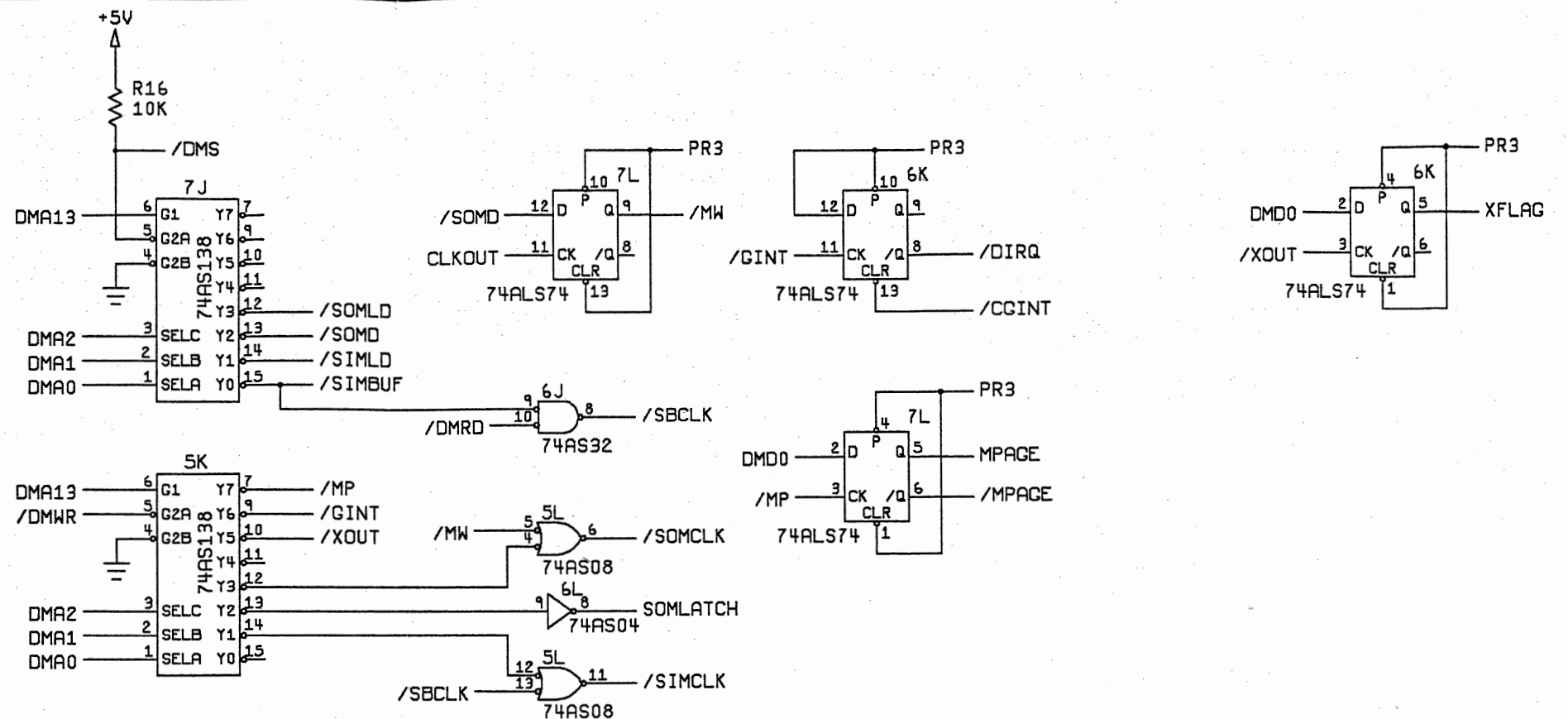
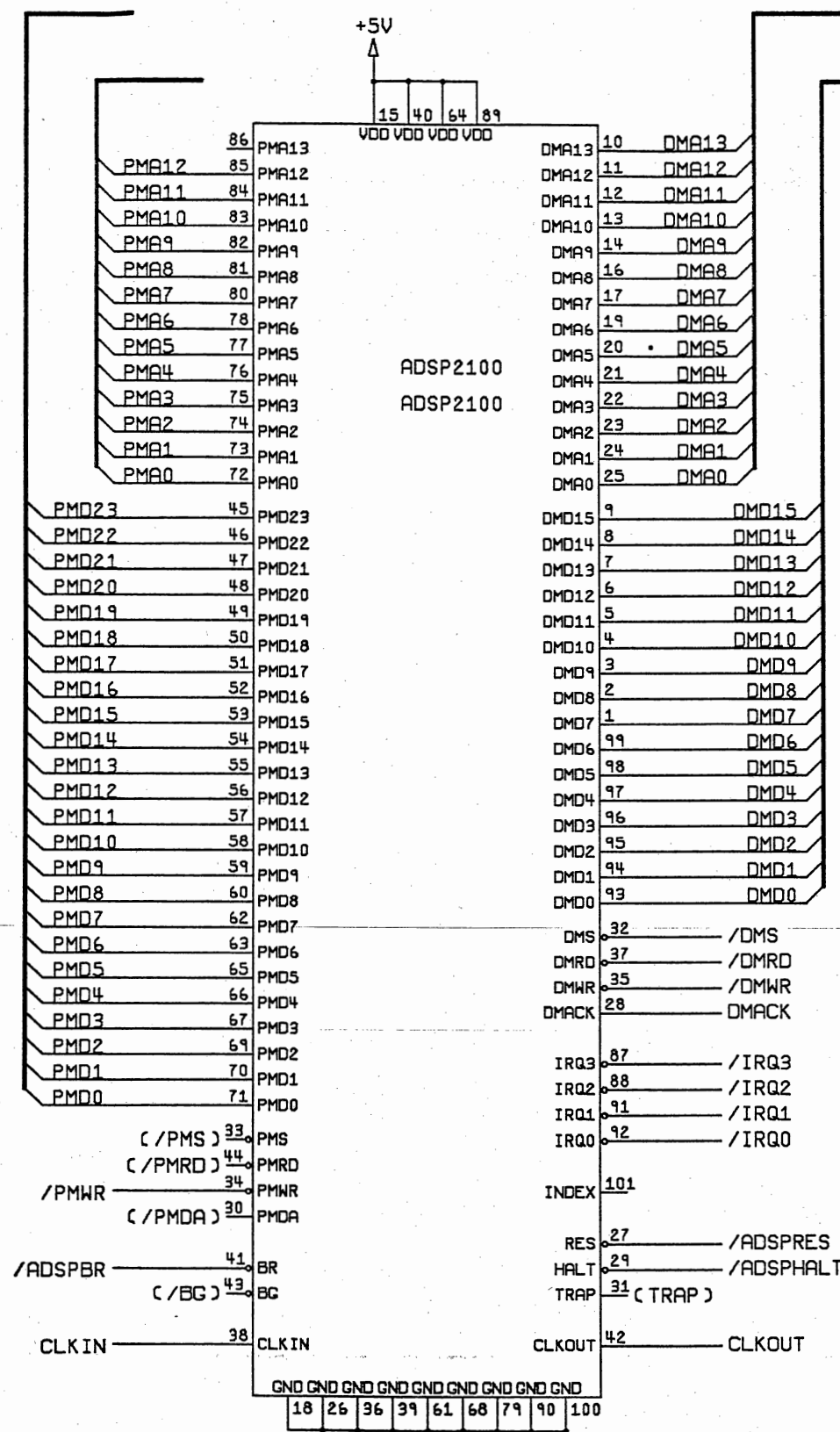
IC TYPE	GND	VCC
74LS00	7	14
74LS08	7	14
74LS175	8	16
74LS244	10	20
74LS245	10	20
74LS253	8	16
74LS259	8	16
74LS373	10	20
74LS374	10	20
74ALS20	7	14
74ALS32	7	14
74ALS74	7	14
74ALS138	8	16
74ALS169	8	16
74ALS569	10	20
74AS00	7	14
74AS04	7	14
74AS08	7	14
74AS32	7	14
74AS74	7	14
74AS138	8	16
4K X 4 SRAM	10	20
8K X 8 SRAM	14	28
27512	14	28
ADSP2100	18 26 36 39 61 68 79 90 100	15 40 64 89

	1	2	3	4	5	6	7	8	9	10	11	12	13
N	25 DMA0	27 RESET	29 HALT	31 TRAP	33 PMS	36 GND	39 GND	40 VDD	43 BG	45 PMD23	47 PMD21	48 PMD20	50 PMD18
M	23 DMA2	26 GND	28 DMACK	30 PMDA	32 DMS	35 DMWR	37 DMRD	41 BR	44 PMRD	46 PMD22	49 PMD19	51 PMD17	52 PMD16
L	22 DMA3	24 DMA1				34 PMWR	38 CLK1	42 CLK0				53 PMD15	54 PMD14
K	20 DMA5	21 DMA4										55 PMD13	56 PMD12
J	18 GND	19 DMA6										57 PMD11	58 PMD10
H	15 VDD	16 DMA8	17 DMA7									59 PMD9	60 PMD8
G	14 DMA9	12 DMA11	13 DMA10									63 PMD6	62 PMD7
F	11 DMA12	10 DMA13	9 DMA15									67 PMD3	66 PMD4
E	8 DMD14	7 DMD13										69 PMD2	68 GND
D	6 DMD12	5 DMD11										71 PMD0	70 PMD1
C	4 DMD10	3 DMD9	INDEX PIN			92 IRQ0	88 IRQ2	84 PMA11				74 PMA2	72 PMA0
B	2 DMD8	1 DMD7	99 DMD6	96 DMD3	94 DMD1	91 IRQ1	87 IRQ3	85 PMA12	82 PMA9	80 PMA7	78 PMA6	76 PMA4	73 PMA1
A	100 GND	98 DMD5	97 DMD4	95 DMD2	93 DMD0	90 GND	89 VDD	86 PMA13	83 PMA10	81 PMA8	79 GND	77 PMA5	75 PMA3

ADSP - 2100
PIN LOCATIONS

BOTTOM VIEW
(PINS UP)

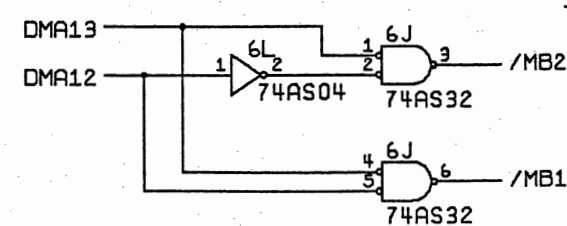
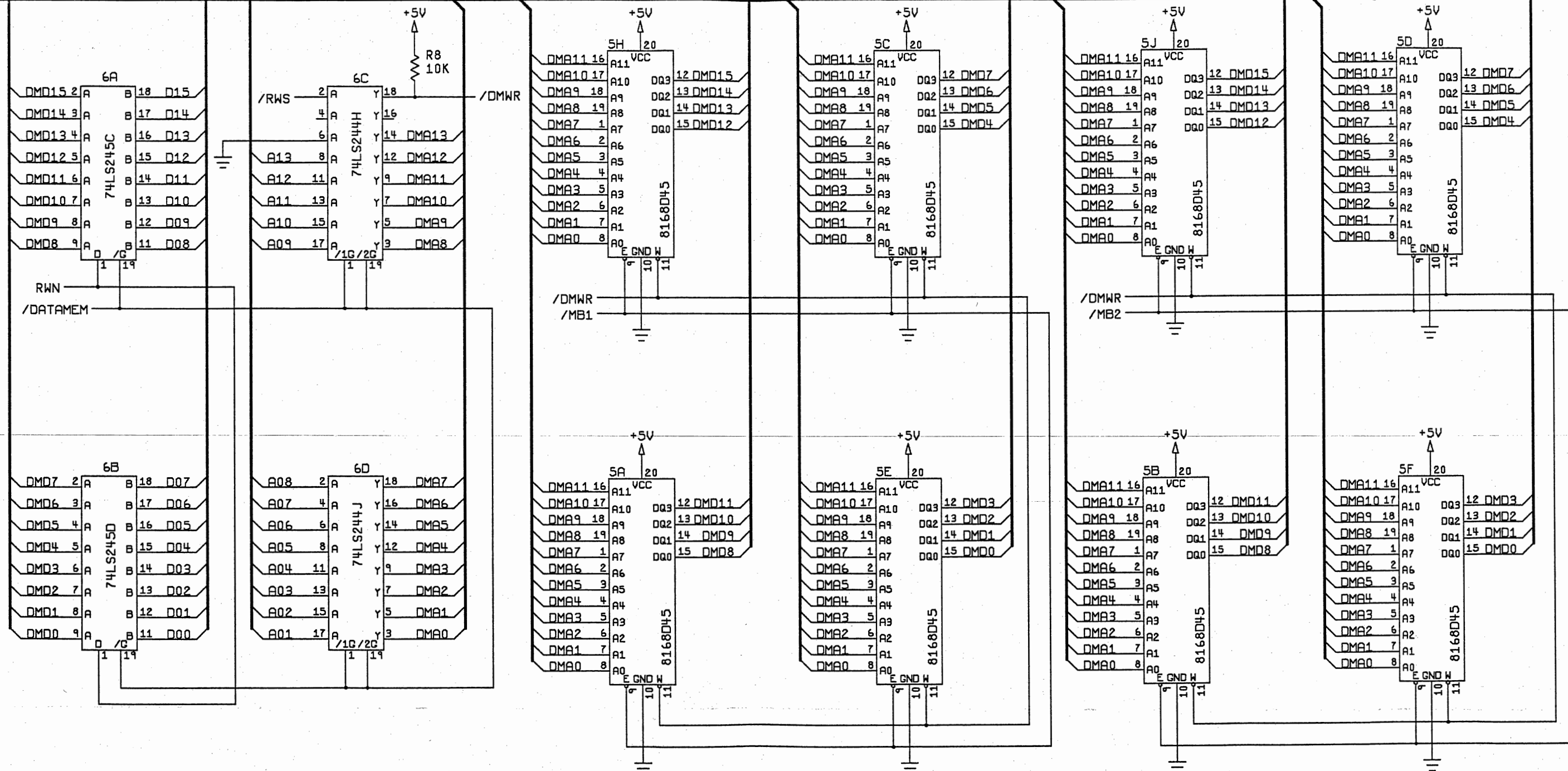
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		CHECKED BY C.D. DATE 8-2-88	
TOLERANCES ON: ANGLES ± 1° .XX ± .01 .XXX ± .005		ENGR/ELECT R. Menden DATE 8-2-88	
MATERIAL: SEE PL A045739-01		MFP ENGR R. Menden DATE 8-3-88	
FINISH:			
A044421-21 DRIVING SIMULATOR		ATARI	
NEXT ASSY FIRST USED ON		ATARI GAMES CORP. 675 SYCAMORE DRIVE MILPITAS, CA. 95035	
NOTICE TO ALL PERSONS RECEIVING THIS DRAWING CONFIDENTIAL: REPRODUCTION FORWARDED WITHOUT THE SPECIFIC WRITTEN PERMISSION OF ATARI GAMES CORPORATION, HAYWARD, CA. THIS DRAWING IS ONLY CONDITIONALLY ISSUED, AND NEITHER RECEIPT NOR POSSESSION THEREOF CONFERES OR TRANSFERES ANY RIGHT IN, OR LICENSE TO USE, THE SUBJECT MATTER OF THE DRAWING OR ANY DESIGN OR TECHNOLOGY, INFOR- MATION FROM THEREON, NOR ANY RIGHT TO REPRODUCE THIS DRAWING OR ANY PART THEREOF, EXCEPT FOR MANUFACTURE BY HOLDERS OF ATARI GAMES CORPORATION, AND FOR REPRODUCTION UNDER THE CORPORATION'S WRITTEN LICENSE. NO RIGHT IS GRANTED TO REPRODUCE THIS DRAWING OF THE SUBJECT MATTER THEREOF, UNLESS BY WRITTEN PERMISSION WITH OR WRITTEN FORFEITURE FROM THE CORPORATION.		TITLE SCHEMATIC DRIVER ADSP	
		SIZE D	
		DRAWING NO. 044421-01	
		REV B	
		SCALE NONE	
		SHEET 1 OF 9	



(CONTROL 1 CONNECTED ONLY WITH SIGNAL /ADSPIRQ
(CONTROL 2 CONNECTED ONLY WITH SIGNALS D00 THRU D03)

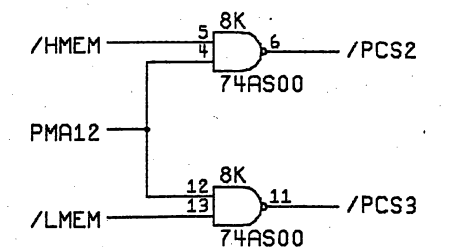
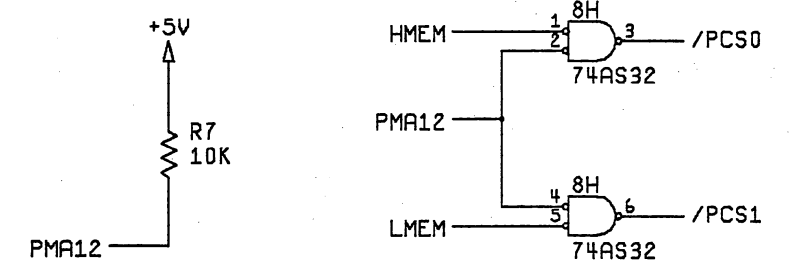
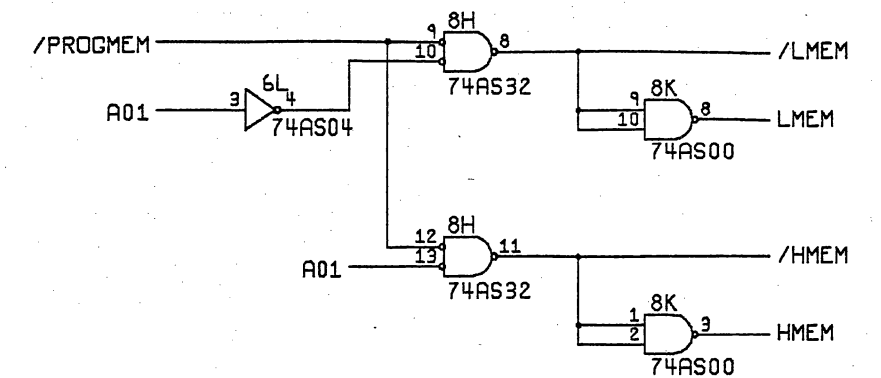
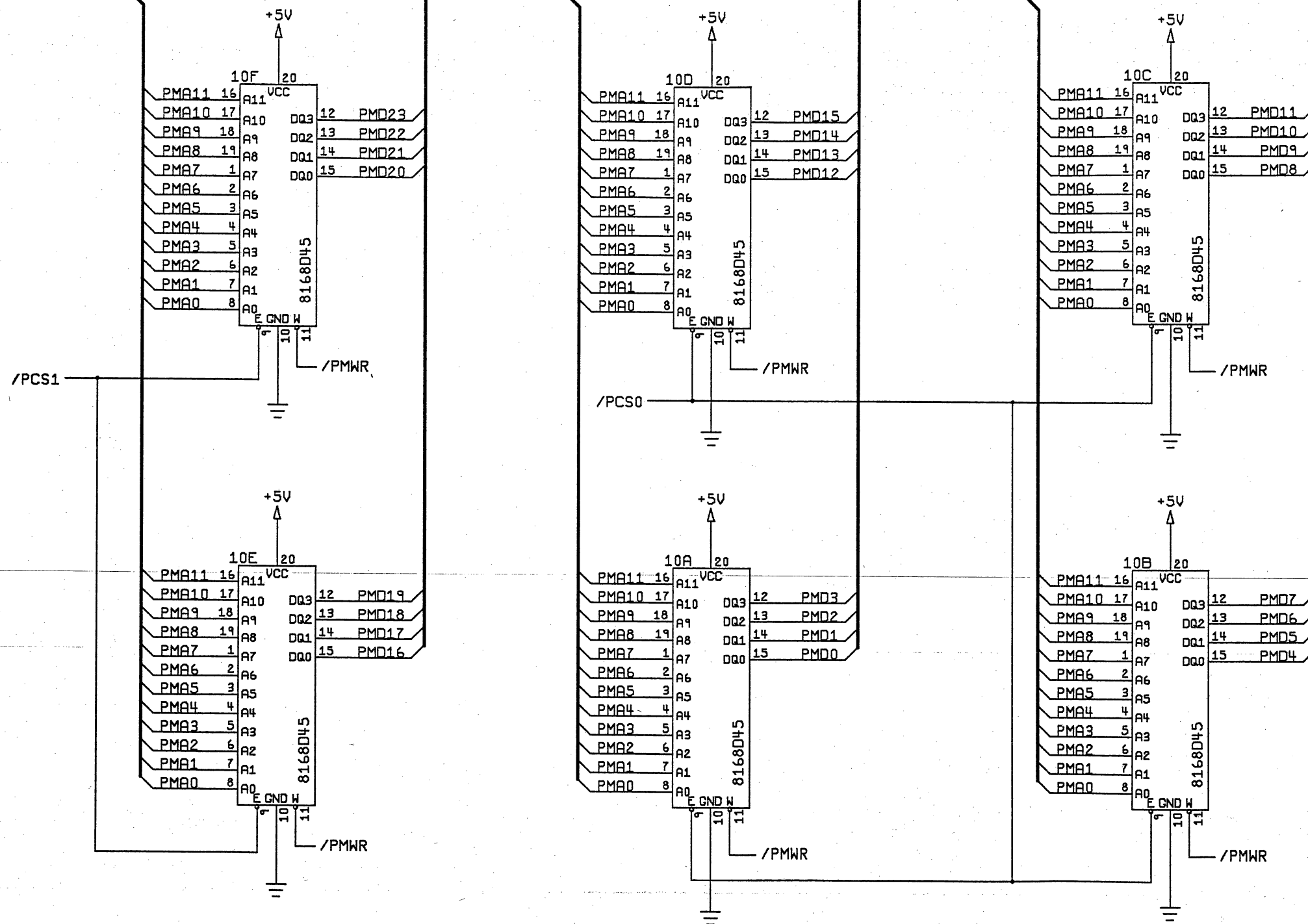
XTAL OSC

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SCALE NONE		SHEET 3 OF 9	



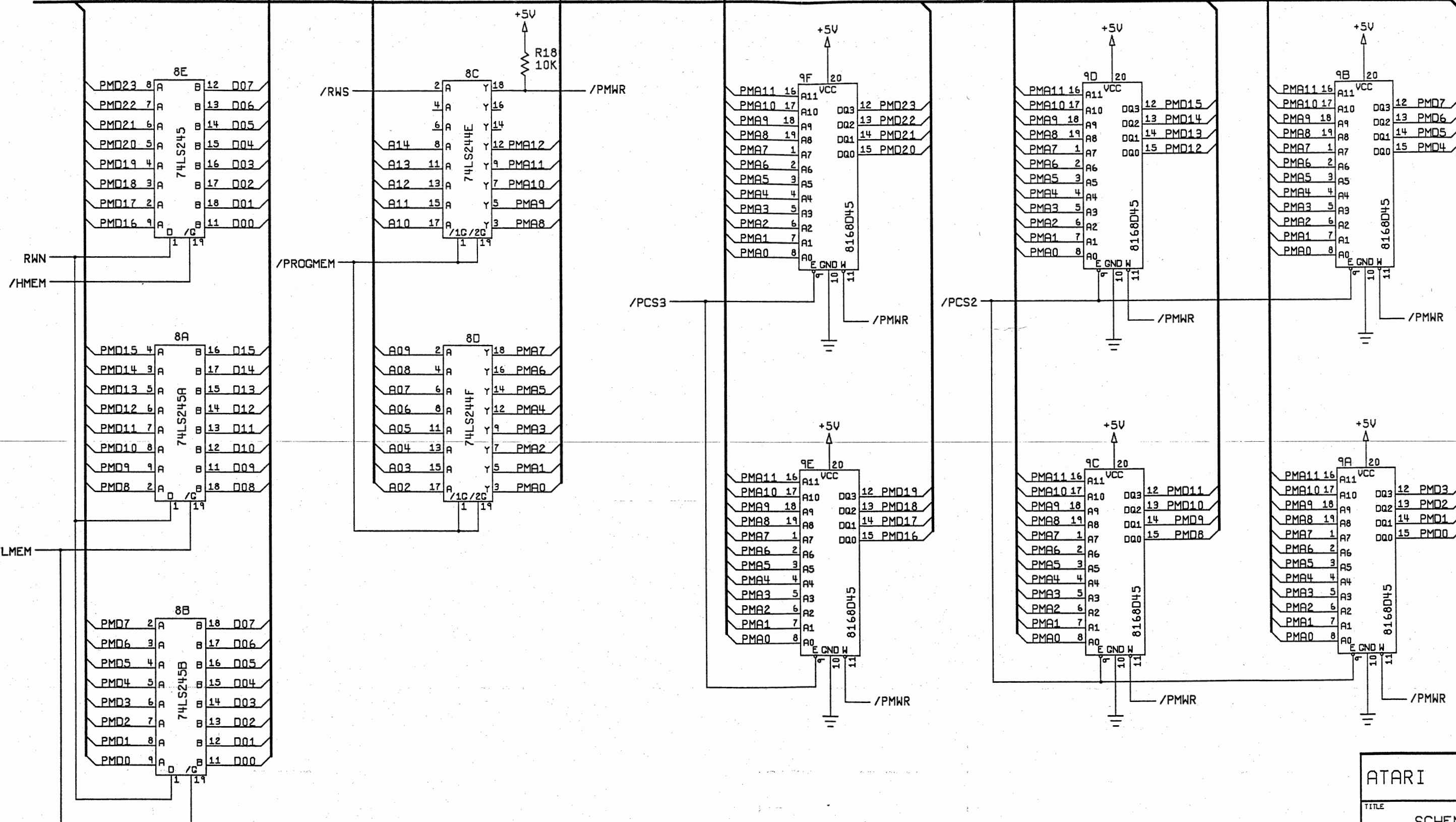
DATA MEMORY

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ATARI GAMES CORP. 675 SYCAMORE DRIVE MILPITAS, CA. 95035		
TITLE		
SCHEMATIC DRIVER ADSP		
SIZE	DRAWING NO.	REV
D	044421-01	B
SCALE	NONE	SHEET 4 OF 9



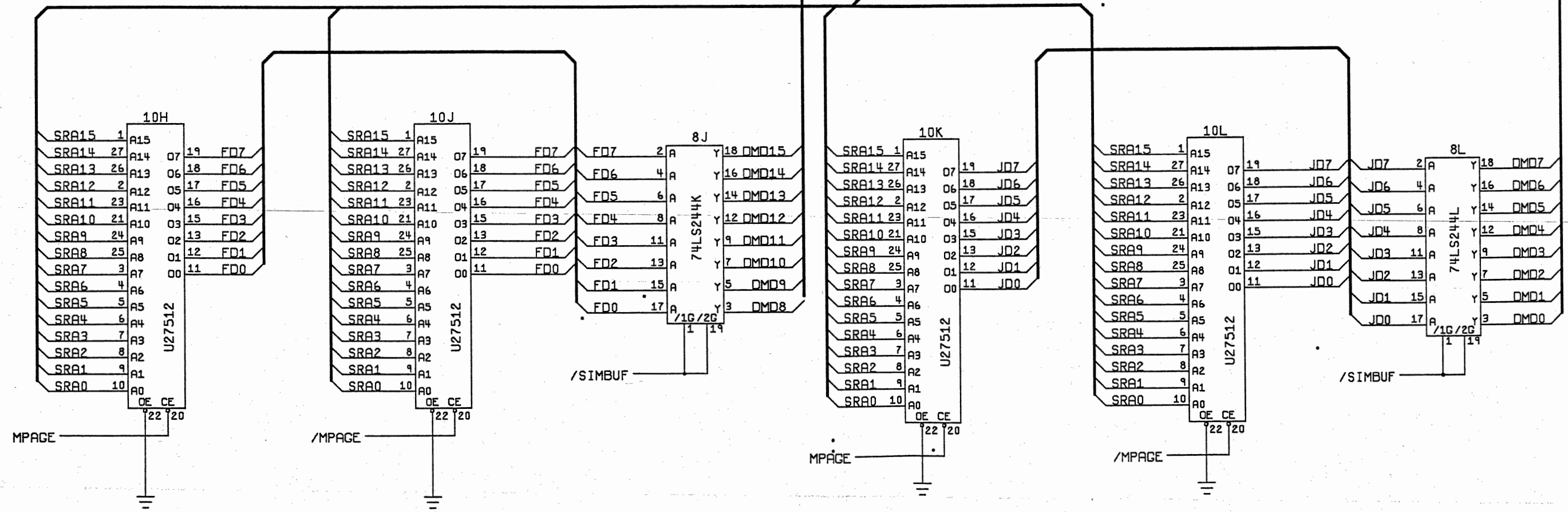
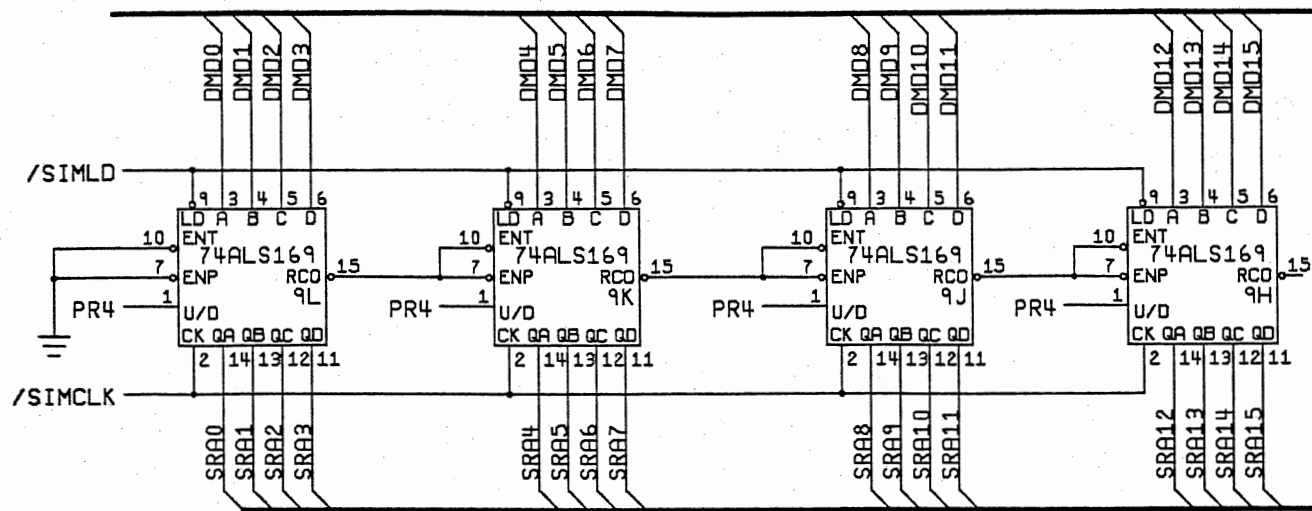
PROGRAM MEMORY

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TITLE SCHEMATIC DRIVER ADSP			
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SCALE NONE		SHEET 5 OF 9	



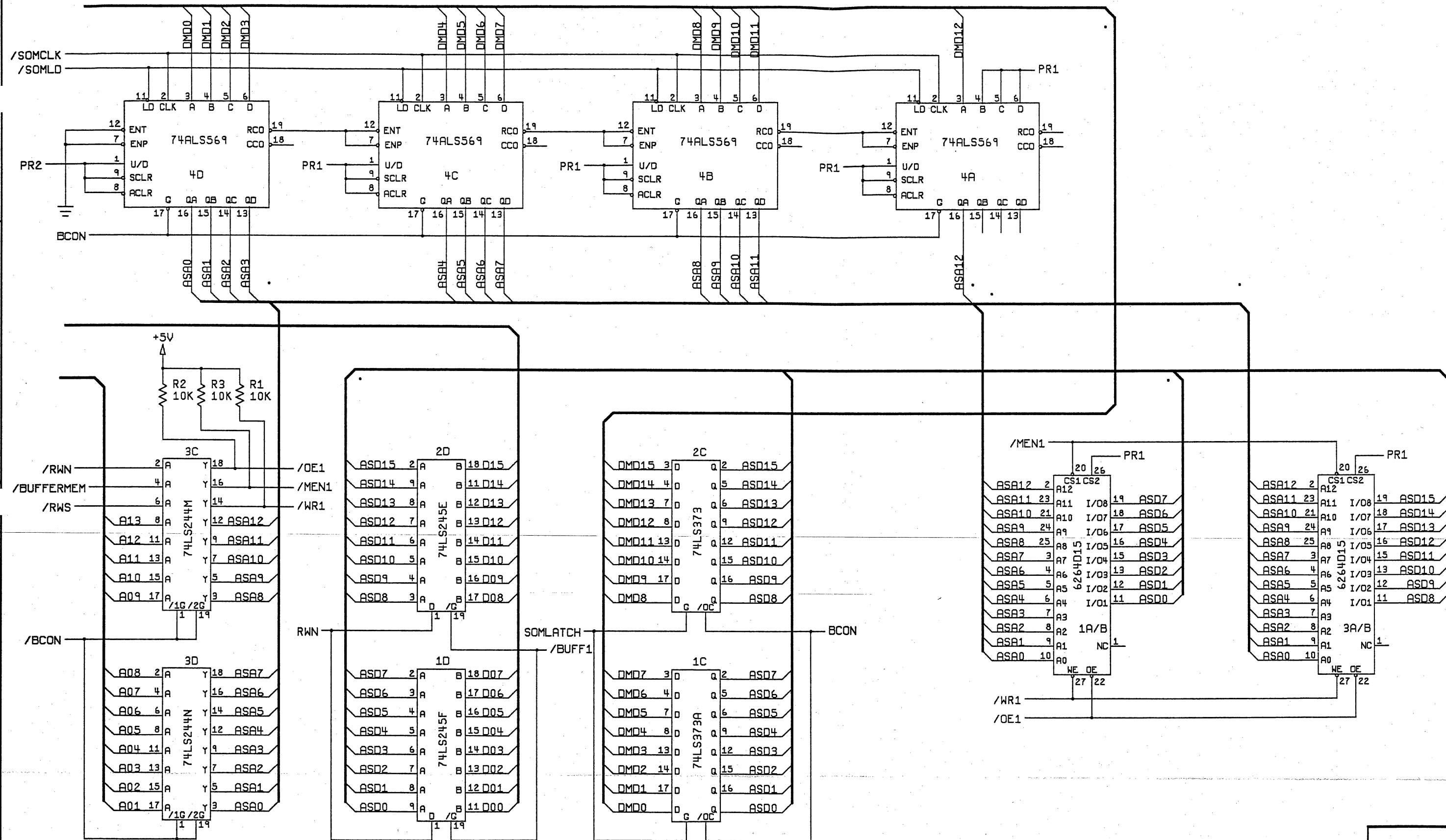
PROGRAM MEMORY /BUFFERS

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TITLE SCHEMATIC DRIVER ADSP			
SIZE D	DRAWING NO. 044421-01	REV B	
SCALE NONE	SHEET 6 OF 9		



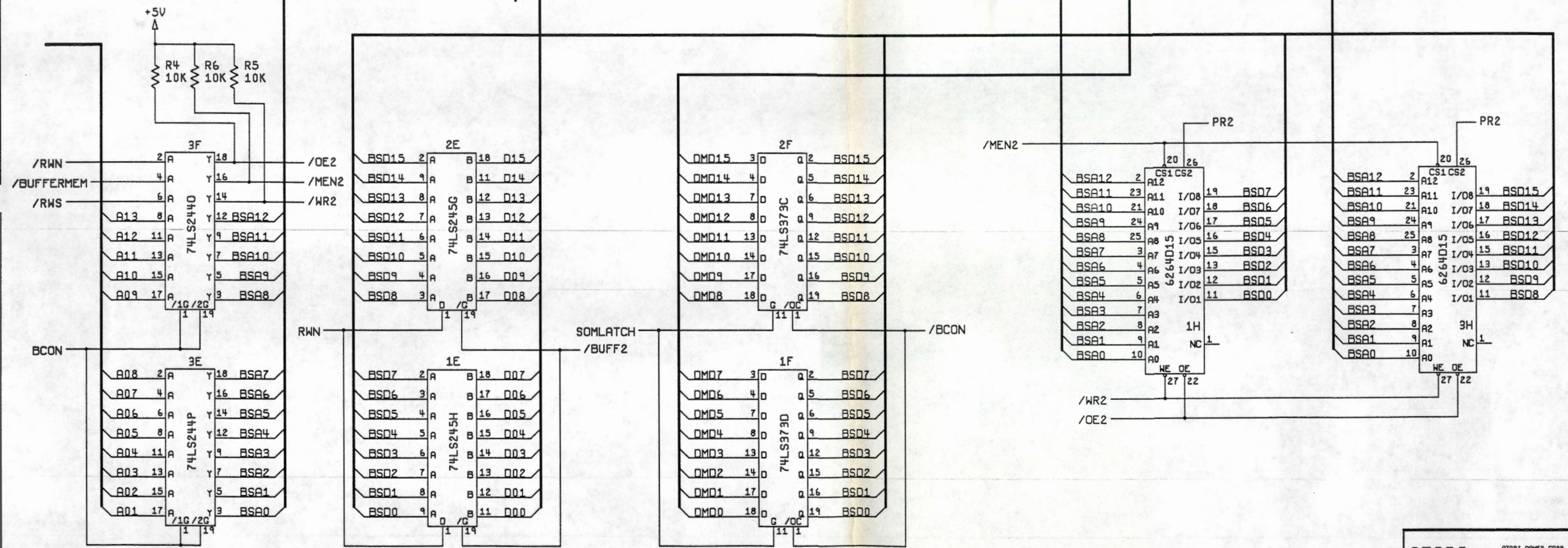
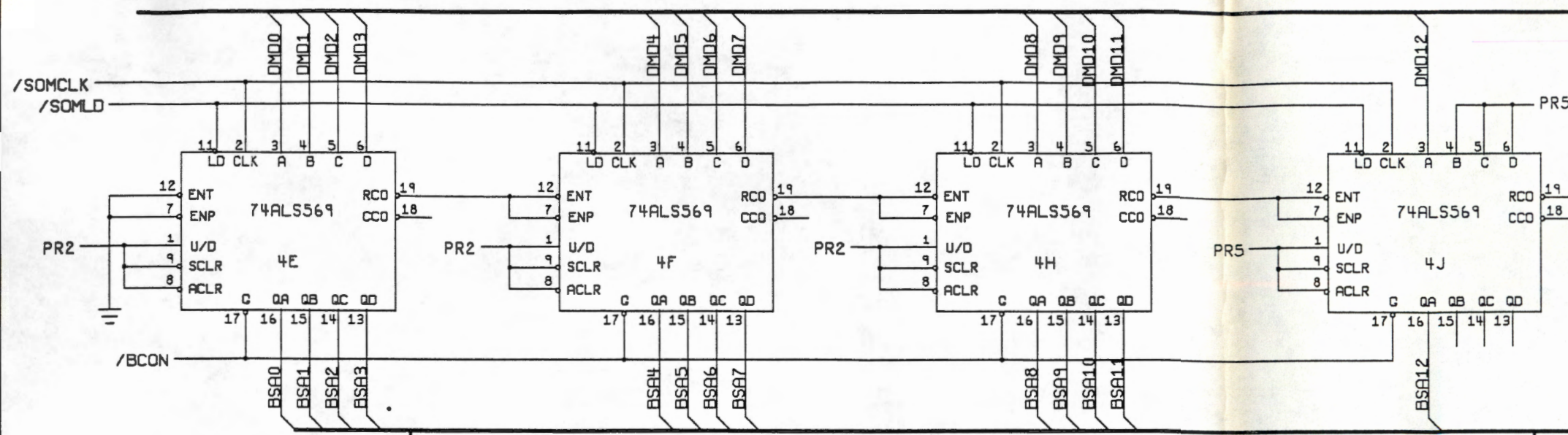
SEQUENTIAL INPUT MEMORY

ATARI		ATARI GAMES CORP. 675 SYCAMORE DRIVE MILPITAS, CA. 95035	
TITLE			
SCHEMATIC DRIVER ADSP			
SIZE	DRAWING NO.	REV	
D	044421-01	B	
SCALE	NONE	SHEET	7 OF 9



SEQUENTIAL OUTPUT MEMORY #1

ATARI		
ATARI GAMES CORP. 675 SYCAMORE DRIVE MILPITAS, CA. 95035		
TITLE		
SCHEMATIC DRIVER ADSP		
SIZE	DRAWING NO.	REV
D	044421-01	B
SCALE	NONE	SHEET 8 OF 9



SEQUENTIAL OUTPUT MEMORY #2

ATARI		
ATARI GAMES CORP. 675 SYCAMORE DRIVE MILPITAS, CA. 95035		
TITLE		
SCHEMATIC DRIVER ADSP		
SIZE	DRAWING NO.	REV
D	044421-01	B
SCALE	NONE	SHEET 9 OF 9

Tab - “ADSP II”

Title / ASSY, SUB, ADSP II PCB		P/L A047047-01	Rev / C
GAMES ENGINEERING		PROJECT: H.D.	
PARTS LIST SPECIFICATION		Page 1 of 2	



Drawn by: L. FRITTS	Next Assy:
Checked by:	A047046-01,02
Design Eng:	Comp. Eng:
Proj. Eng:	Mfg. Eng:
Ind. Design:	Qual. Eng:

REV	DESCRIPTION	DATE	APPR	REV	DESCRIPTION	DATE	APPR
A	PRODUCTION REL	6/89					
B	REVISED PER ECN 13811	4/90					
C	REVISED PER ECN 13954	8-10-90	JM				

ITEM	PART NO	QTY	Description	Ref. Designators
1	047048-01	1	P.C. Board	
2				
3				
4				
5	122002-104	94	CAP, .1μF, 50V, CER	C2-95
6	124008-107	1	CAP, 100μF, 16V, ELEC	C1
7				
8				
9				
10	179021-060	1	CONN, HDR, 60 CKT .2 CTR	J1
11				
12				
13				
14	131027-002	3	DIODE, MV5053, LIGHT EMIT	CR1-3
15				
16				
17				
18	144008-002	1	IC, 32MHZ CLOCK MODULE	X1
19	137517-001	2	IC, 74ALS138	7B, 7C
20	137464-001	1	IC, 74ALS32	7A
21	137476-001	8	IC, 74ALS569	4A, 4B, 4C, 4D, 4E, 4F, 4H, 4J
22	137156-001	2	IC, 74ALS74	6K, 7L
23	137480-001	1	IC, 74AS00	8K
24	137433-001	1	IC, 74AS04	6L
25	137484-001	1	IC, 74AS08	5L
26	137522-001	2	IC, 74AS138	5K, 7J
27	137487-001	2	IC, 74AS32	6J, 8H
28	137097-001	1	IC, 74LS139	8/9J
29	137038-001	13	IC, 74LS244	3C, 3D, 3E, 3F, 3K, 6C, 6D, 7D, 8C, 8D, 8F, 8L, 8H/J
30	137134-001	9	IC, 74LS245	1D, 1E, 2D, 2E, 6A, 6B, 8A, 8B, 8E
31	137137-001	1	IC, 74LS259	7K
32	137143-001	4	IC, 74LS373	1C, 1F, 2C, 2F
33	137537-003	20	IC, SRAM, 4KX4, 45 NS	5A, 5B, 5C, 5D, 5E, 5F, 5H,

Title / ASSY, SUB, ADSP II PCB

P/L A047047-01

REV / C

GAMES ENGINEERING

PROJECT: H.D.

PARTS LIST SPECIFICATION

Page 2 of 2

ITEM	PART NO	QTY	Description	Ref. Designators
34	137471-001	4	IC, 74ALS169	5J, 9A, 9B, 9C, 9D, 9E, 9F, 10A, 10B, 10C, 10D, 10E, 10F 8/9K, 8/9L, 8/9F/H, 8/9H/J
35	137535-004	4	IC, RAM, 8KX8, 100 NSEC	1H, 3H, 1A/B, 3A/B
36				
37	110000-103	15	RES, 10K, 5%, 1/4W	R1-12, R16-18
38	110000-151	2	RES, 150, 5%, 1/4W	R13, R14
39	110000-102	7	RES, 1K, 5%, 1/4W	R19-23, R48, R49
40	110000-221	1	RES, 220, 5%, 1/4W	R15
41				
42				
43				
44	179257-028	6	SOCKET, 28 PIN, .600"	9H, 9K, 10H, 10K, 9/10H, 9/10K
45	179288-001	1	HOUSING, SOCKET, PQFP, 100PIN	ADSP2100
46				
47				
48	179051-001	6	TEST POINT	+5V1, +5V2, GND1-4

Title / ASSY, ADSP II PCB		P/L A047046-02	Rev / B
GAMES ENGINEERING PARTS LIST SPECIFICATION		PROJECT: H.D. COMPACT	Page 1 of 1



Drawn by: L. FRITTS	Next Assy:
checked by: J.D. 6-21-89	
Design Eng: J. MARGOLIN 6-21-89	Comp. Eng:
Proj. Eng:	Mfg. Eng: D.W. 6-22-89
Ind. Design:	Qual. Eng:

REV	DESCRIPTION	DATE	APPR	REV	DESCRIPTION	DATE	APPR
A	PRODUCTION REL	6/89	JM				
B	ECN 13597						

ITEM	PART NO	QTY	Description	Ref. Designators
1	A047047-01	1	ASSY, SUB, ADSP II PCB	
2				
3				
4				
5	137629-001	1	IC, ADSP-2100, 16 BIT DSP, PQFP	ADSP2100
6	179288-002	1	COVER, IC, PQFP, 100 PIN	ADSP2100
7	136052-1136	1	IC, OTP, 27C512-250, 137454-250	9/10K
8	136052-1135	1	IC, OTP, 27C512-250, 137454-250	9/10H
9	136052-1138	1	IC, OTP, 27C512-250, 137454-250	10K
10	136052-1137	1	IC, OTP, 27C512-250, 137454-250	10H

Title / ASSY, ADSP II PCB		P/L A047046-03	Rev / C
GAMES ENGINEERING PARTS LIST SPECIFICATION		PROJECT: H.D. THE RACE	Page 1 of 1



Drawn by: L.FRITTS	Next Assy:
Checked by: J.D. 6-21/89	
Design Eng:	Comp. Eng:
Proj. Eng:	Mfg. Eng:
Ind. Design:	Qual. Eng:

REV	DESCRIPTION	DATE	APPR	REV	DESCRIPTION	DATE	APPR
A	PRODUCTION RELEASE						
B	ECN 14023						
C	ECN 14067 6-7-10-26-90	10-30-90	JM				

ITEM	PART NO	QTY	Description	Ref. Designators
1	A047047-01	1	ASSY, SUB, ADSP II PCB	
2				
3				
4				
5	137629-001	1	IC, ADSP-2100, 16 BIT DSP, PQFP	ADSP2100
6	179288-002	1	COVER, IC, PQFP, 100 PIN	ADSP2100
7	136077-2021	1	IC, EPROM, 27512, 250NS, 137448-250	9/10H
8	136077-2022	1	IC, EPROM, 27512 250NS, 137448-250	10H
9	136077-2023	1	IC, EPROM, 27512 250NS, 137448-250	9/10K
10	136077-2024	1	IC, EPROM, 27512, 250NS, 137448-250	10K

Title / ASSY, ADSP II PCB		P/L A047046-04	Rev / A
GAMES ENGINEERING		PROJECT: RACE DRIVIN PANORAMA	
PARTS LIST SPECIFICATION		Page 1 of 1	

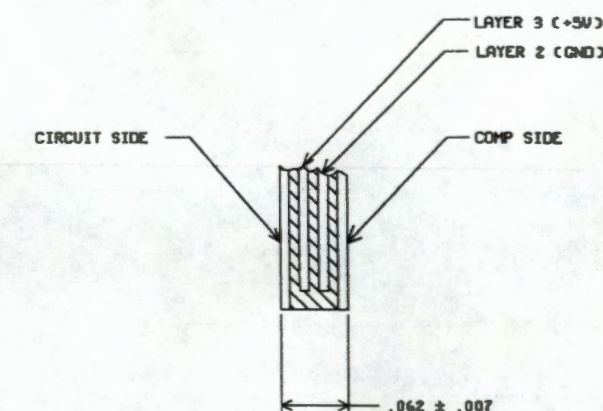
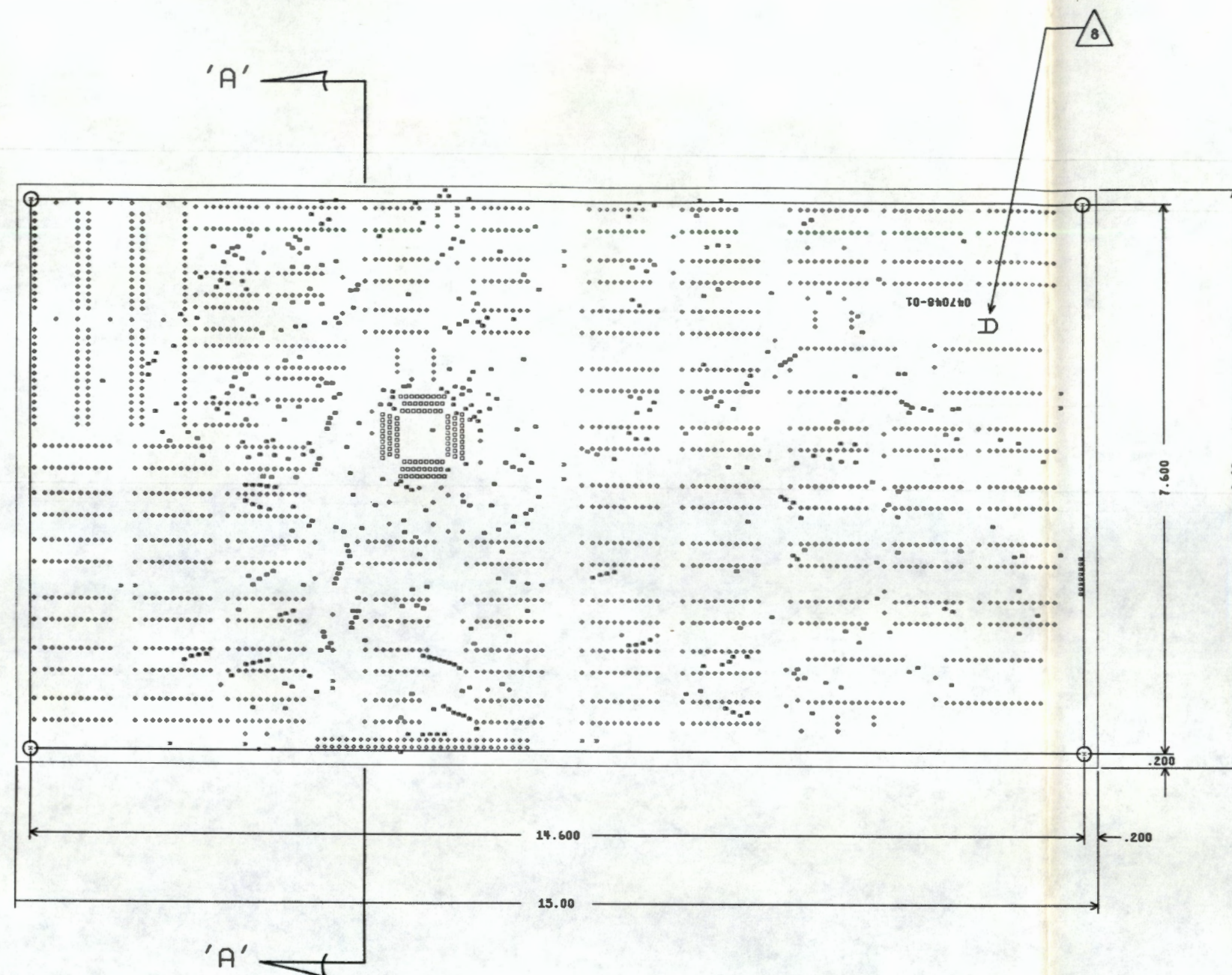


Drawn by: STAFF	Next Assy:
Checked by: <i>L. B. Fitch</i> 4-1-91	
Design Eng:	Comp. Eng:
Proj. Eng: <i>J. Margolin</i> 4-1-91	Mfg. Eng: <i>[Signature]</i> 4-1-91
Ind. Design:	Dual. Eng:

REV	DESCRIPTION	DATE	APPR	REV	DESCRIPTION	DATE	APPR
A	PRODUCTION RELEASE	4-1-91	<i>gm</i>				

ITEM	PART NO	QTY	Description	Ref. Designators
1	A047047-01	1	ASSY, SUB, ADSP II PCB	
2				
3				
4				
5	137629-001	1	IC, ADSP-2100, 16 BIT DSP, PQFP	ADSP2100
6	179288-002	1	COVER, IC, PQFP, 100 PIN	ADSP2100
7				
8	136088-1017	1	IC, EPROM, 27512, 200NS, 137448-200	9/10K
9	136088-1018	1	IC, EPROM, 27512, 200NS, 137448-200	9/10H
10				
11	136088-1019	1	IC, EPROM, 27512, 200NS, 137448-200	10K
12	136088-1020	1	IC, EPROM, 27512, 200NS, 137448-200	10H
13				
14	136088-1021	1	IC, EPROM, 27512, 200NS, 137448-200	9K
15	136088-1022	1	IC, EPROM, 27512, 200NS, 137448-200	9H

REVISIONS					
SYN	DESCRIPTION	DATE	INCRP	CHECK	APPROVED
A	PRODUCTION REL.	6-21-89	LEF	JD	JM



SECTION 'A-A'

SCALE: NONE

DRILL TABLE CHART			
SYMBOL	FINISHED DIA	QTY	PLATED THRU
◇	.040 ± .003	2068	YES
A	.047 ± .003	24	YES
B	.028 ± .003	442	YES
□	.026 ± .002	100	YES
H	.191 ± .003	4	YES

NOTES:

1. MATERIAL: BASE LAMINATE, COPPER CLAD GLASS BASE, EPOXY RESIN, FLAME RETARDANT, 1 OZ COPPER ON ALL INTERNAL LAYERS, 1 OZ COPPER ON EXTERNAL LAYERS SHALL BE IN ACCORDANCE WITH MIL-P-55617. BONDING AGENT: PRE-IMPREGNATED-B STAGE (UNCURED RESIN SHEET) SHALL BE IN ACCORDANCE WITH IPC-L-110.
2. PLATING: SOLDER PLATE, INCLUDING PC FINGERS (CONNECTOR).
3. MAX. TWIST OF WARP PERMITTED IS .005 PER INCH.
4. VENDOR LOGO TO BE ADDED TO BOARD IN CLEAR AREA.
5. SOLDERMASK BOARD WITH PC-401 OR EQUIV, BOTH SIDES.
6. FABRICATE PER ATARI PC BOARD MANUFACTURING SPECIFICATION 190012.
7. SILK SCREEN COMPONENT SIDE OF BOARD USING PERMANENT-TYPE YELLOW EPOXY INK.

8. CURRENT REVISION LEVEL OF FILM TO FABRICATE BOARD TO BE SHOWN ON CIRCUIT SIDE.
9. AS VIEWED FROM THE COMPONENT SIDE, LAYER SEQUENCE NUMBERS MUST READ IN ORDER 'COMP, 2, 3, CIRCUIT'.
10. TOOLING HOLES TO BE CLEAR OF SOLDERMASK .50 DIA., 4PLCS.
11. BOARD TO BE FABRICATED USING 'FINE LINE' TECHNOLOGY. MAXIMUM OVER-ETCH ALLOWED .0020. MAXIMUM UNDER-ETCH ALLOWED .0010.
12. ALL BOARDS TO BE 100% ELECTRICALLY TESTED FOR SHORTS AND OPENS.

A047047-01	DRIVER SIMULATOR
NEXT ASSY	FIRST USED ON
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DO NOT SCALE DRAWING	DRAWN BY L. FRITTS	DATE 6-21-89
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CHECKED BY J. DIEU	DATE 6-21-89
TOLERANCES (IN)	ENGR. ELECT	DATE 6-21-89
ANGLES ± 1°	DESIGN	DATE 6-21-89
.XX ± .01	DATE	
.XXX ± .005	DATE	
MATERIAL:	DATE	
SEE NOTE 1.	DATE	
FINISH:	DATE	
SEE NOTE 2.	DATE	

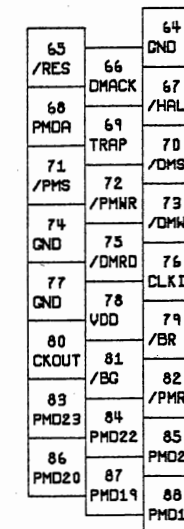
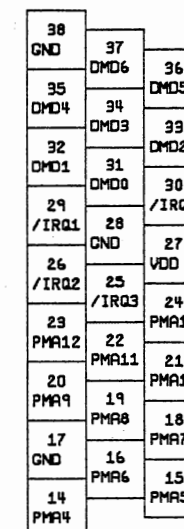


ATARI GAMES CORP.
675 STORMORE DRIVE
MILPITAS, CAL. 95035

TITLE
FABRICATION,
ADSP II PCB

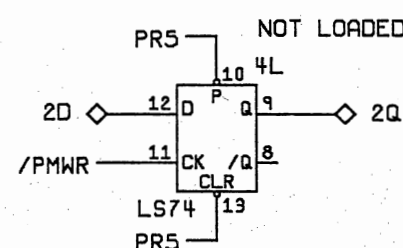
SIZE	DRAWING NO.	REV
D	047048-01	A
SCALE 1:1	SHEET 1 OF 1	

39 DMD7	42 DMD10	45 DMD13	48 DMA13	51 DMA10	54 DMA8	57 DMA6	60 DMA3	63 DMA0
	41 DMD9	44 DMD12	47 DMD15	50 DMA11	53 VOD	56 GND	59 DMA4	62 DMA1
40 DMD8	43 DMD11	46 DMD14	49 DMA12	52 DMA9	55 DMA7	58 DMA5	61 DMA2	



11	8	5	2	99	96	93	90
PMA1	PMD1	PMD3	VDD	GND	PMD10	PMD13	PMD16
12	9	6	3	100	97	94	91
PMA2	PMD0	GND	PMD5	PMD7	PMD9	PMD12	PMD15
13	10	7	4	1	98	95	92
PMA3	PMA0	PMD2	PMD4	PMD6	PMD8	PMD11	PMD14
							89

IC TYPE	GND	VCC
74LS00	1	14
74LS01	1	14
74LS02	1	14
74LS03	1	14
74LS04	1	14
74LS05	1	14
74LS06	1	14
74LS07	1	14
74LS08	1	14
74LS09	1	14
74LS10	1	14
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74LS99	1	14

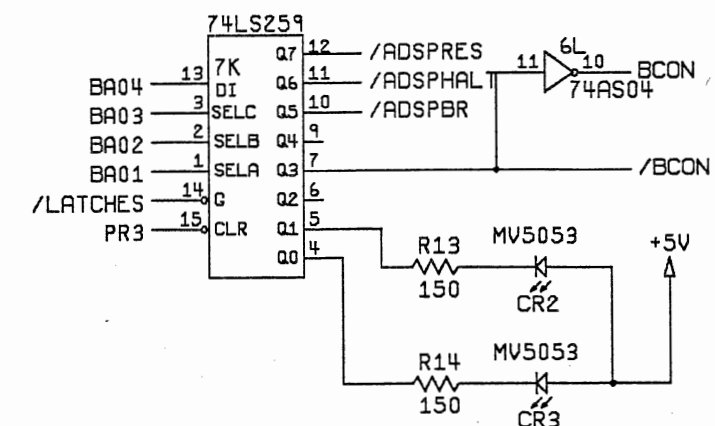
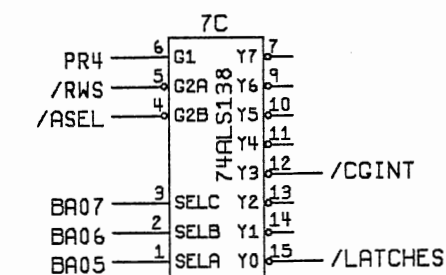
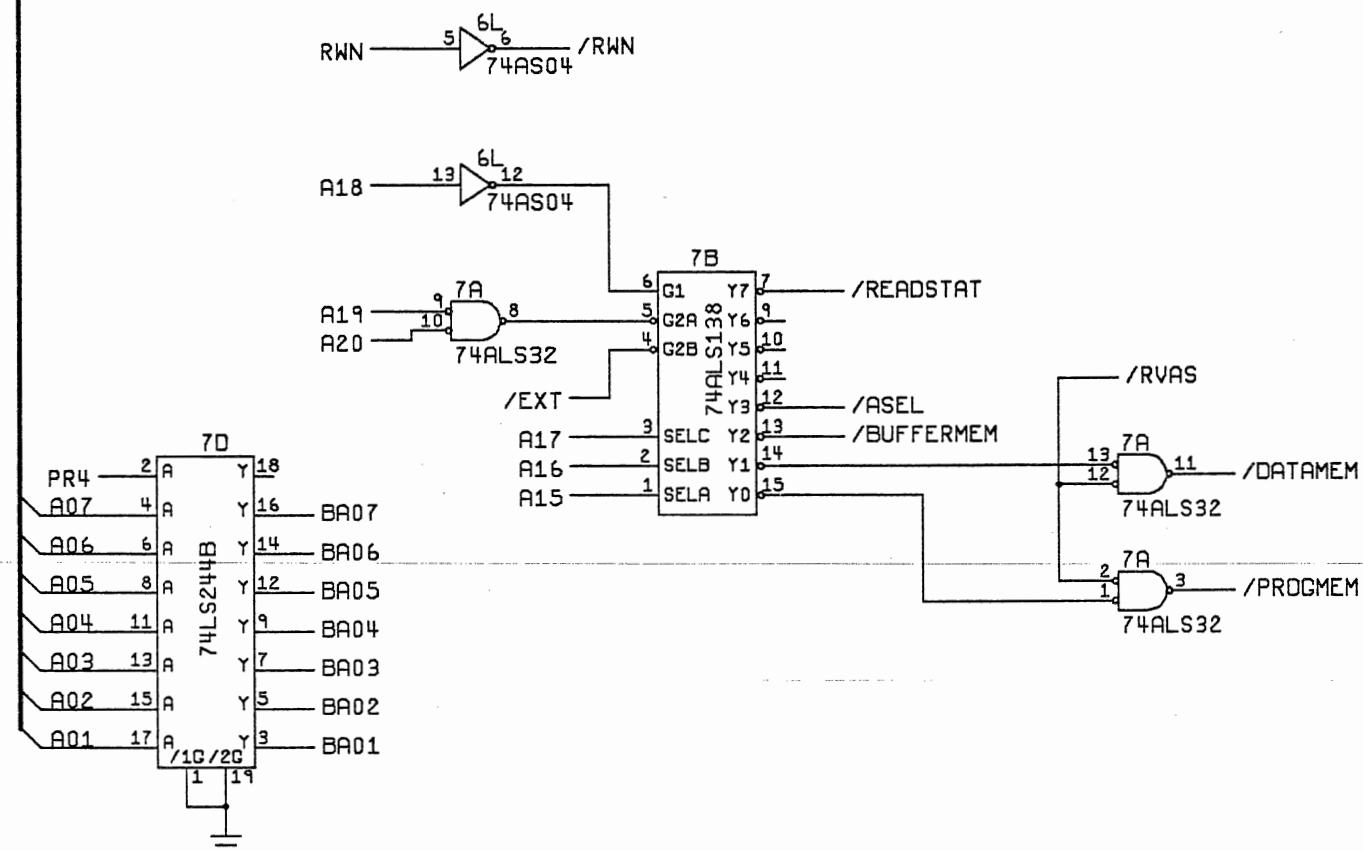
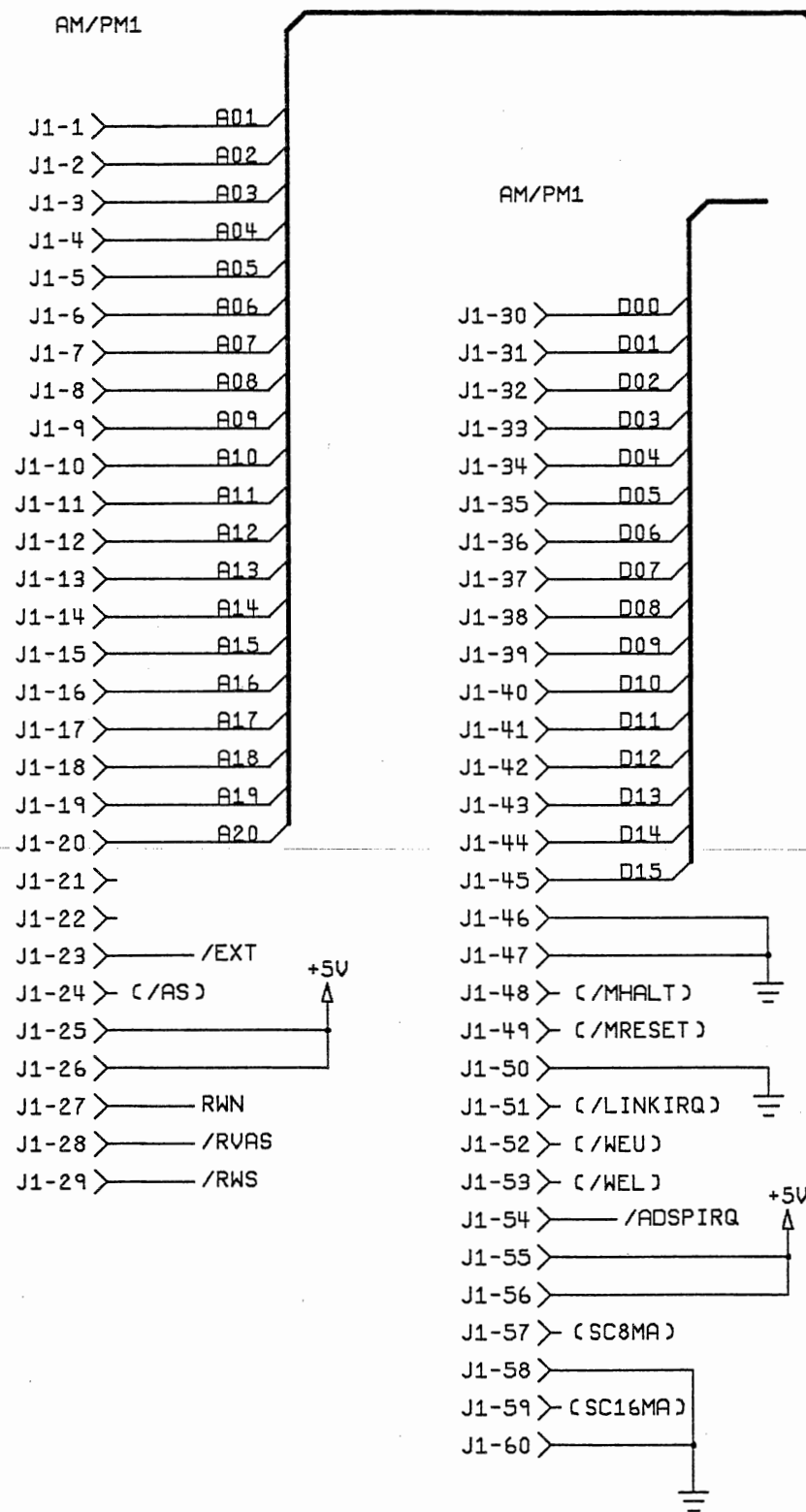


A047047-01	DRIVING SIMULATOR
NEXT ASSY	FIRST USED 0

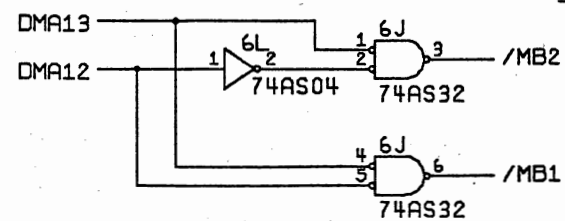
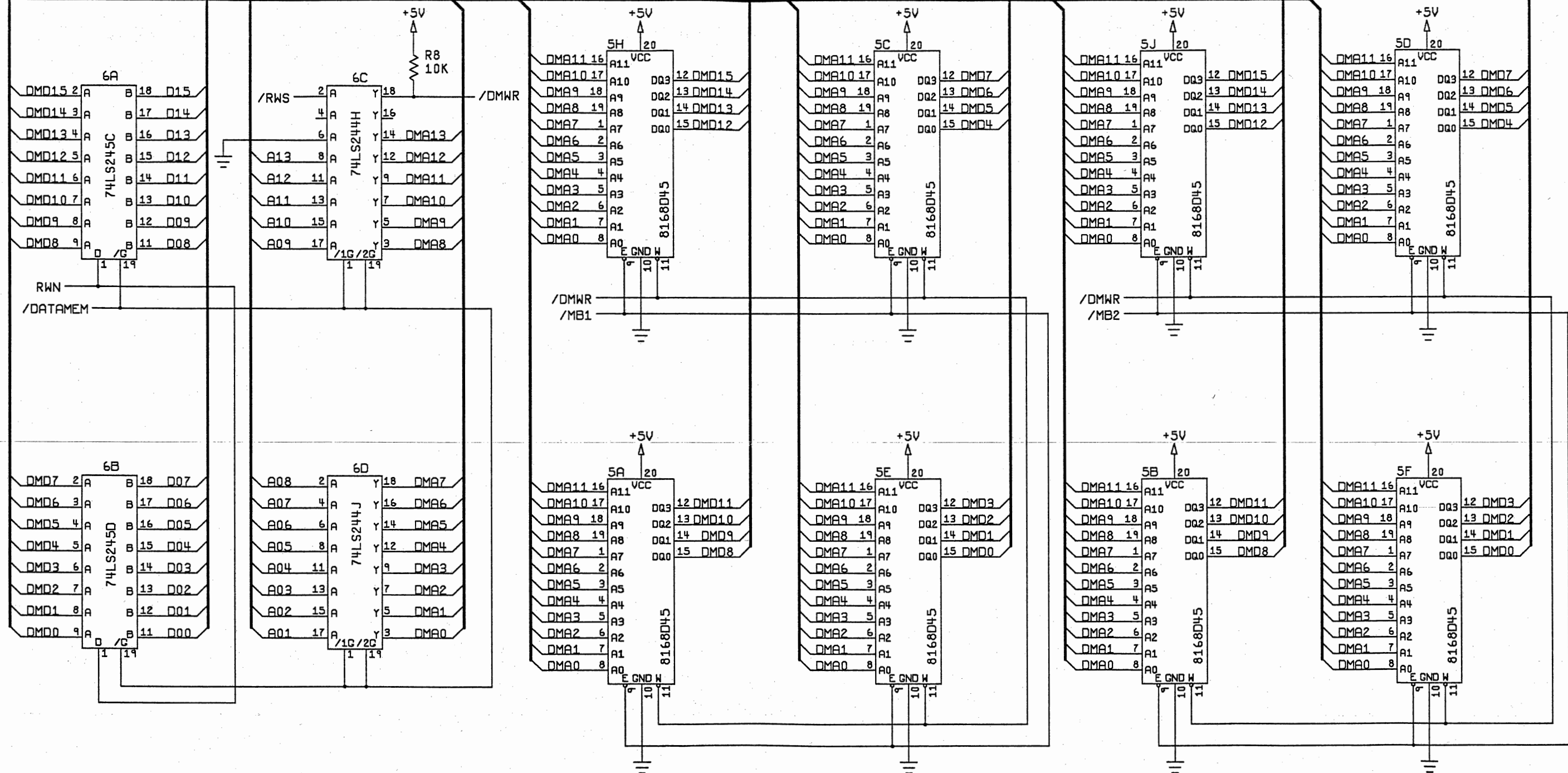
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DO NOT SCALE DRAWING		DRAWN BY L. FRITTS		DATE 6-20-89	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		CHECKED BY JD		DATE 6-21-89	
TOLERANCES ON:		ENGR. ELECT		DATE	
ANGLES $\pm 1^\circ$		A. Mangolin		6-21-89	
.XX \pm .01		PROJ ENGR		DATE	
.XXX \pm .005		MFG ENGR		DATE	
MATERIAL:		ADSP II		6-22-89	
SEE PL A047047-01 A047046-01, -02					
FINISH:					

ATARI		ATARI GAMES CORP. 675 STYACORE DRIVE MILPITAS, CA. 95035	
TITLE		SCHEMATIC ADSP II PCB	
SIZE D	DRAWING NO. 047047-01	REV C	
SCALE NONE	SHEET 1	OF 9	

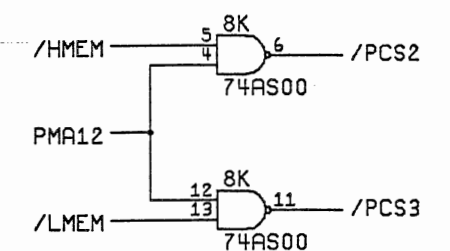
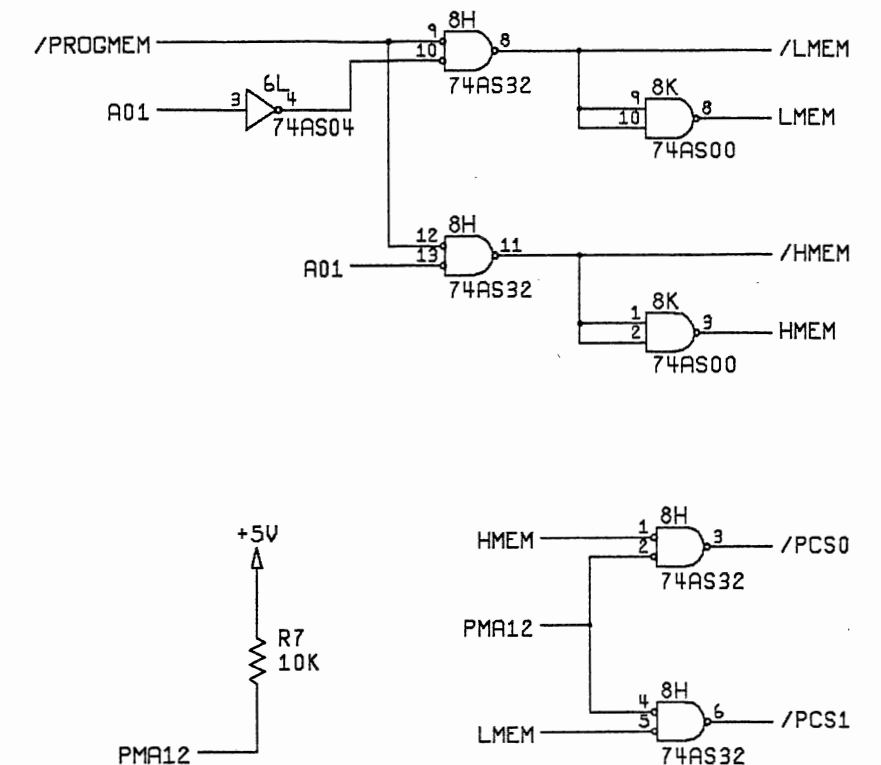
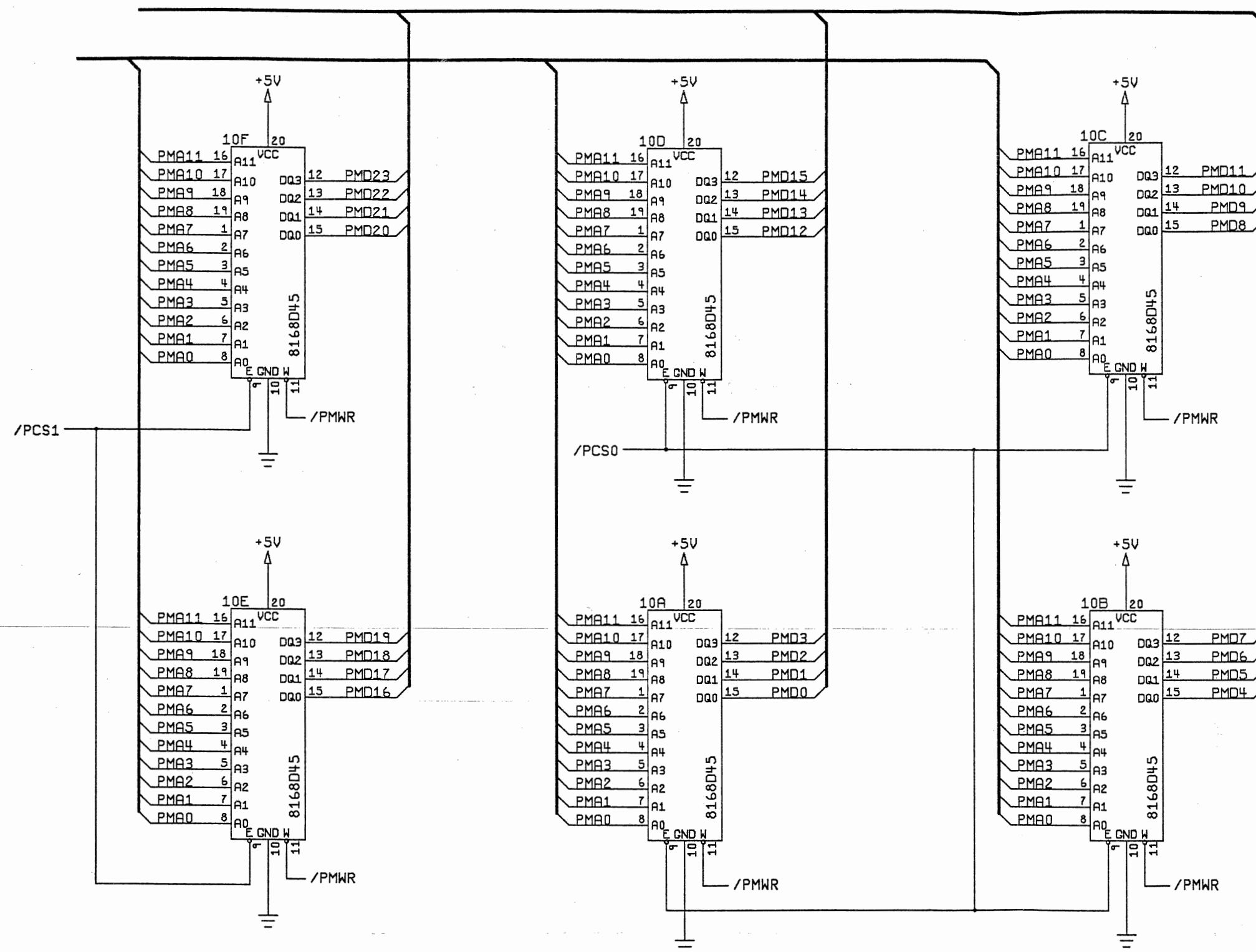


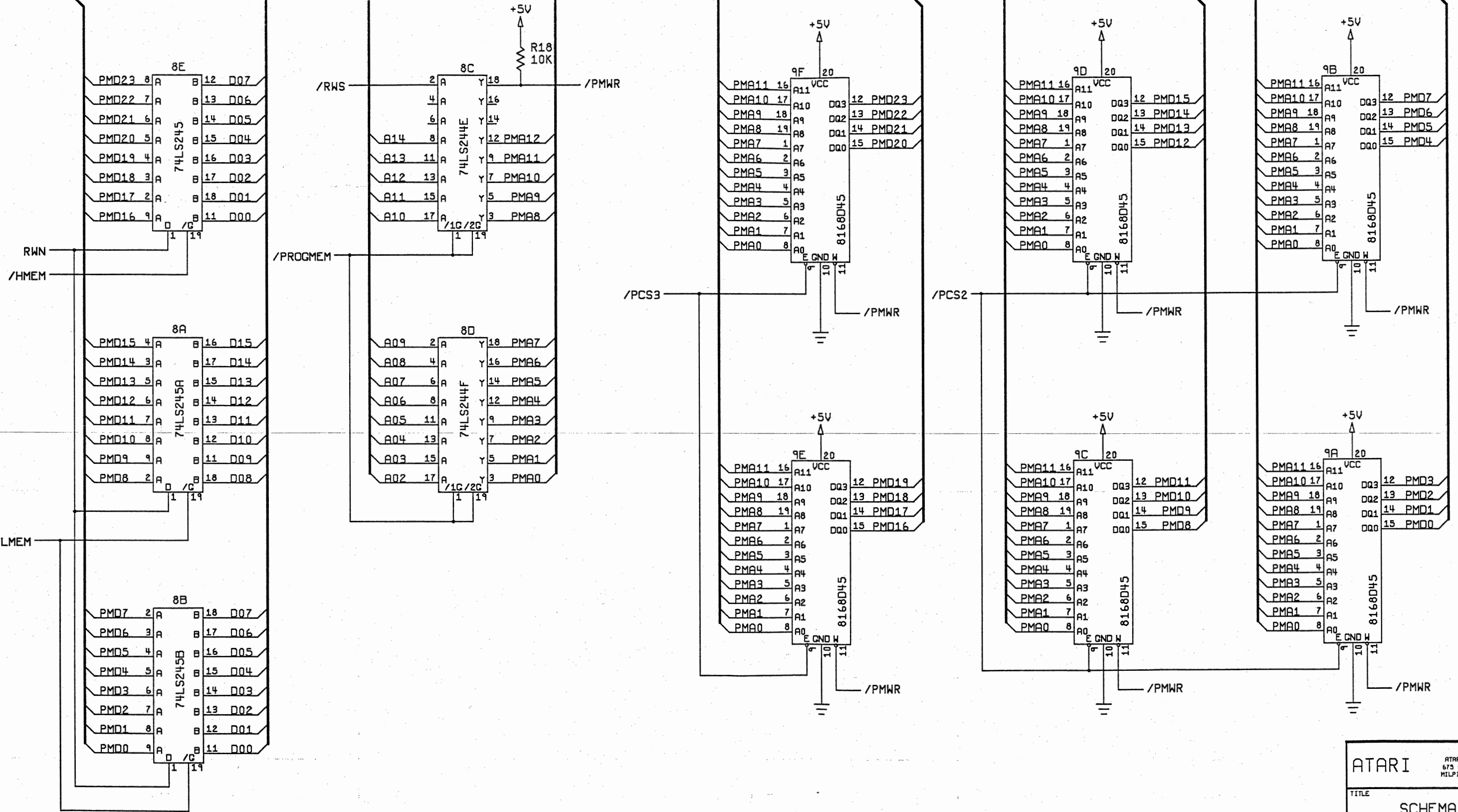
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TITLE		
SCHEMATIC ADSP II PCB		
SIZE	DRAWING NO.	REV
D	047047-01	C
SCALE	NONE	SHEET 2 OF 9



DATA MEMORY

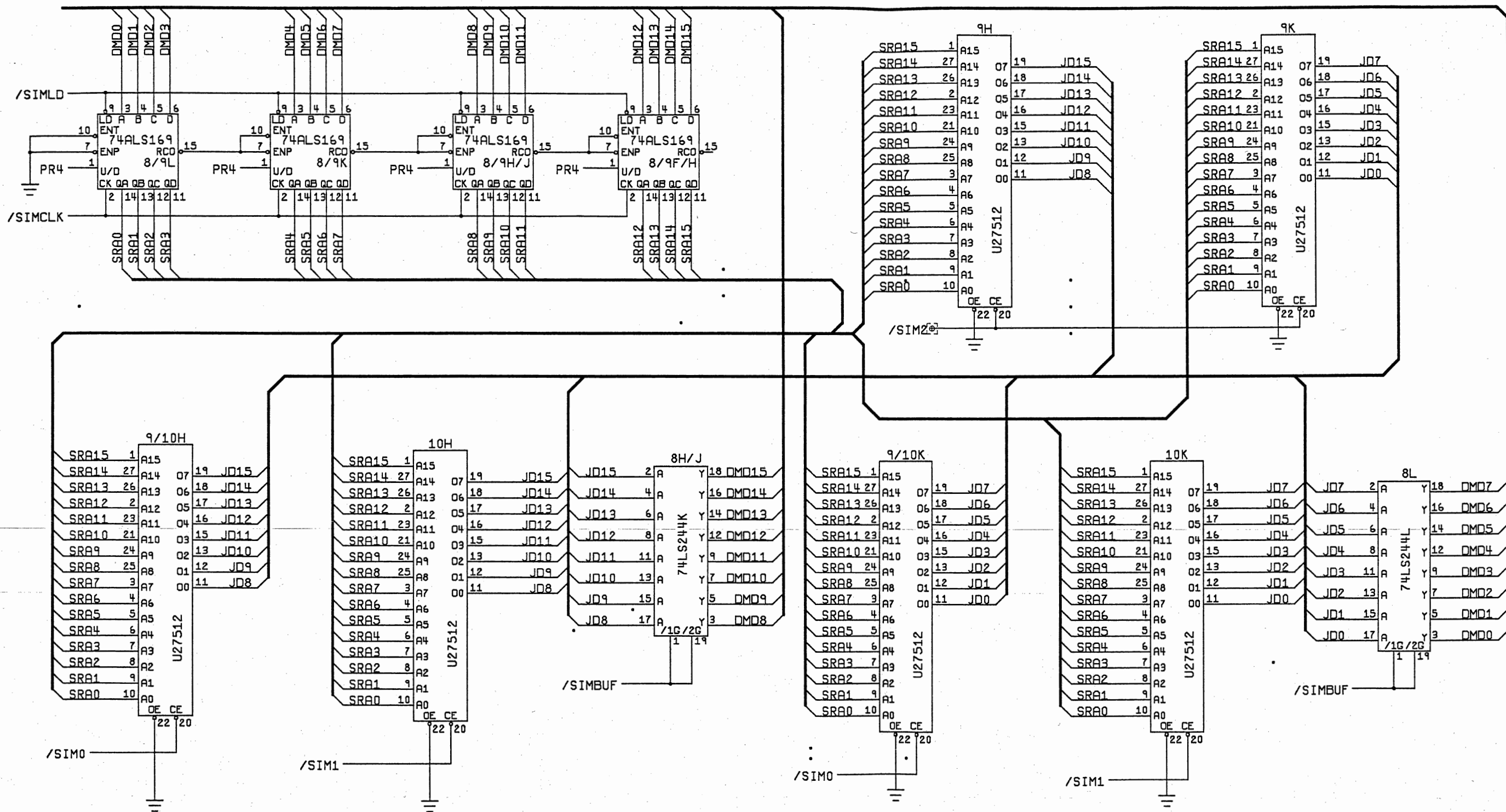
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SCHEMATIC ADSP II PCB		
SIZE	DRAWING NO.	REV
D	047047-01	C
SCALE	NONE	SHEET 4 OF 9





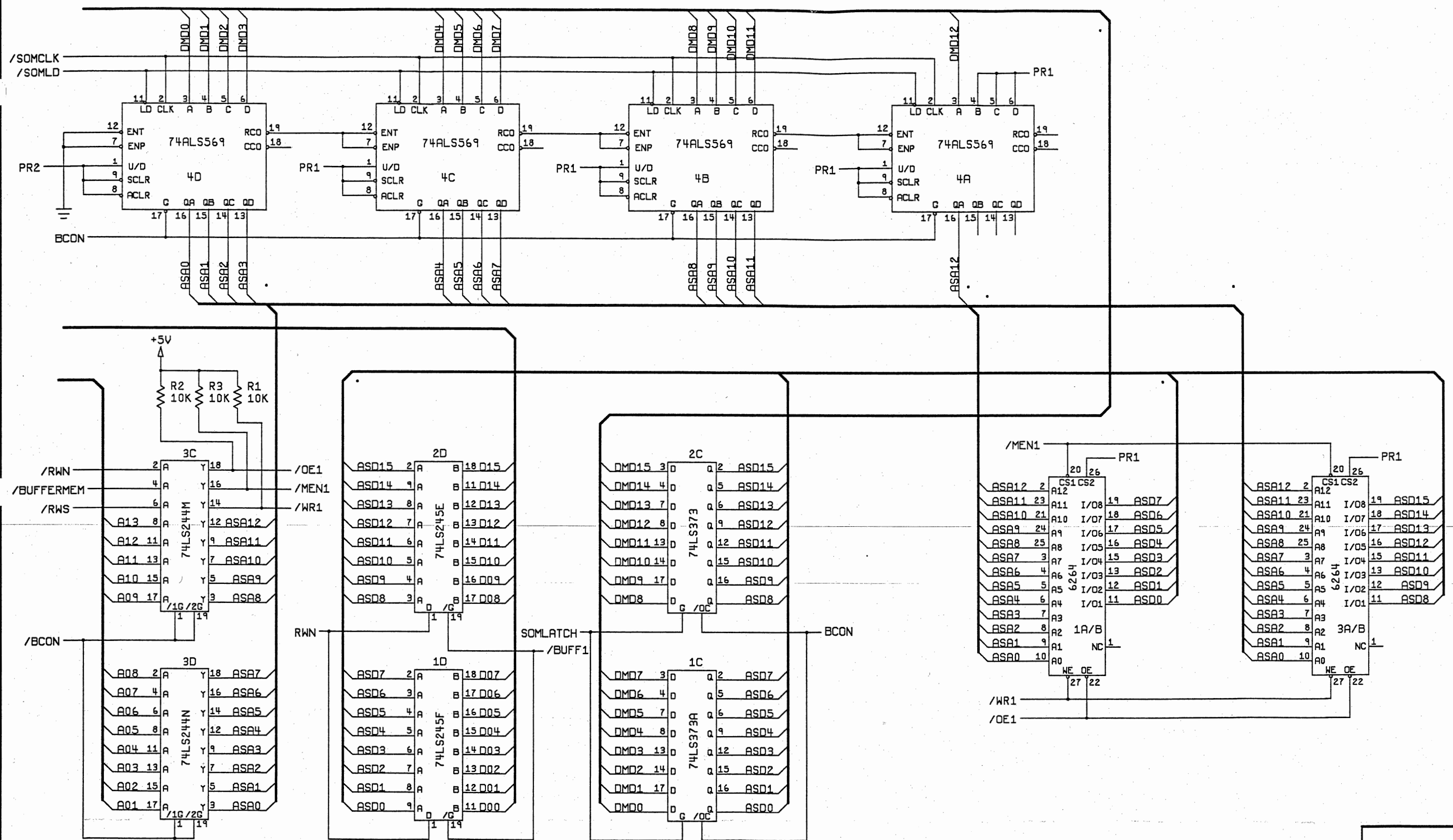
PROGRAM MEMORY /BUFFERS

ATARI		
ATARI GAMES CORP. 675 STICMORE DRIVE MILPITAS, CA. 95035		
TITLE		
SCHEMATIC ADSP II PCB		
SIZE	DRAWING NO.	REV
D	047047-01	C
SCALE	NONE	SHEET 6 OF 9



SEQUENTIAL INPUT MEMORY

ATARI		ATARI GAMES CORP. 675 SYCAMORE DRIVE MILPITAS, CA. 95033
TITLE SCHEMATIC ADSP II PCB		
SIZE D	DRAWING NO. 047047-01	REV C
SCALE NONE	SHEET 7	OF 9



SEQUENTIAL OUTPUT MEMORY #1

ATARI

ATARI GAMES CORP.
675 SYCAMORE DRIVE
MILPITAS, CA. 95035

TITLE

SCHEMATIC
ADSP II PCB

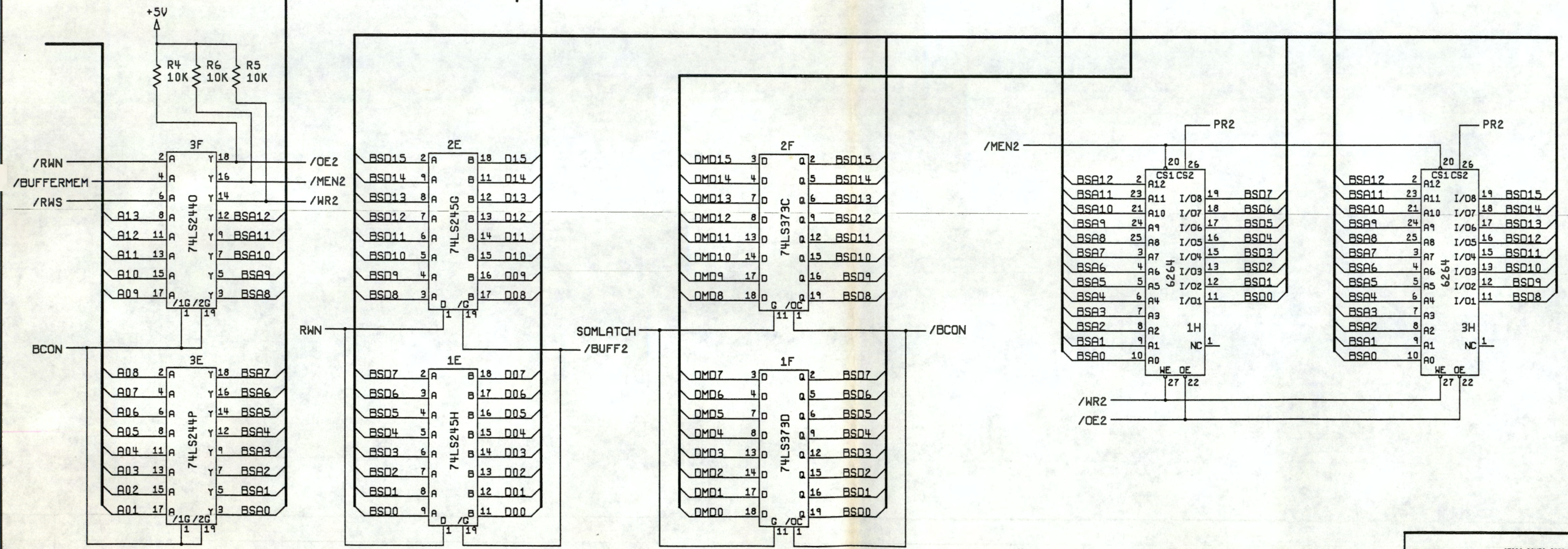
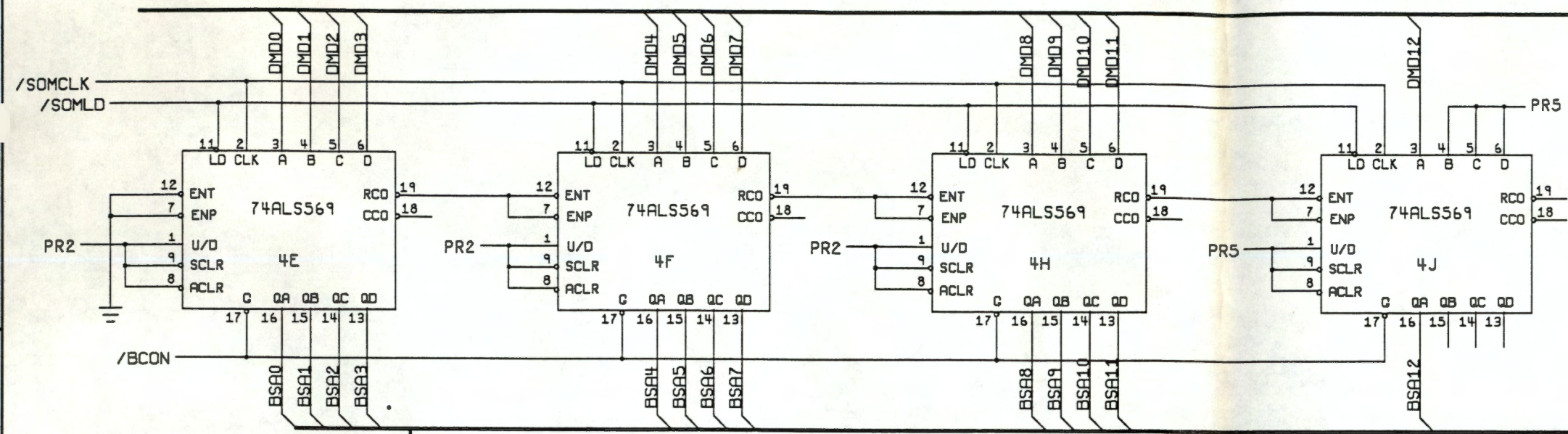
SIZE D

DRAWING NO. 047047-01

REV C

SCALE NONE

SHEET 8 OF 9



SEQUENTIAL OUTPUT MEMORY #2

ATARI		ATARI GAMES CORP. 675 SYCAMORE DRIVE MILPITAS, CA. 95035
TITLE		
SCHEMATIC ADSP II PCB		
SIZE D	DRAWING NO. 047047-01	REV C
SCALE NONE	SHEET 9	OF 9